1. Scope

This specification covers the Electrical Viewfinder with a full color Ferroelectric Liquid Crystal (FLC) display module to be delivered from SONICOM.

2. Specification summary

Table1: Specification summary

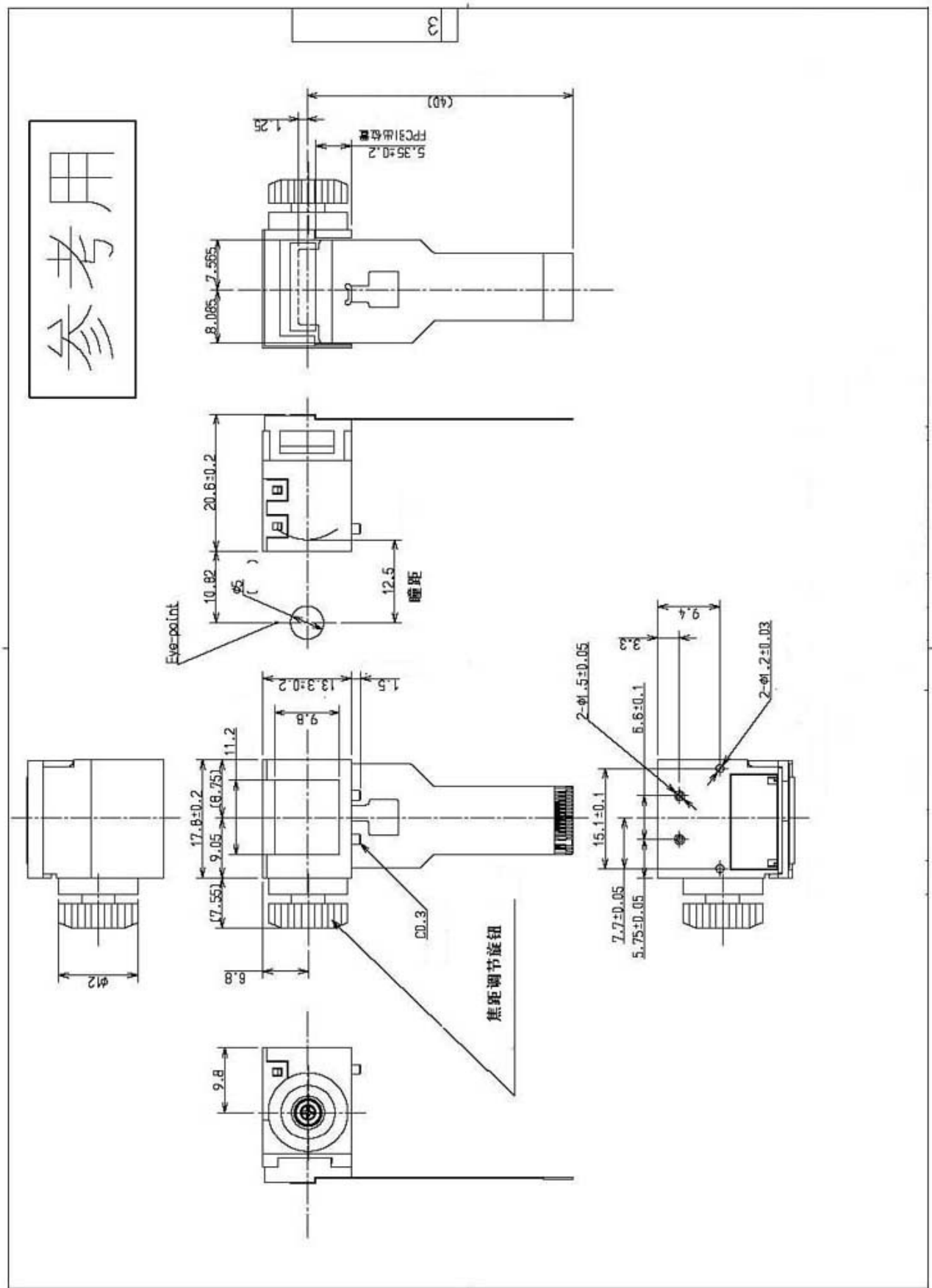
Parameter	Specifications
Display Technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
Display Mode	Field sequential color
Display Format	720(H) x 540(V) *2
Display Panel Active Area	3.96 x 2.97mm *2
Display Area diagonal	4.95mm (0.195") *2
Input Grayscale	256 levels
Color Depth	4.2Million unique colors (YCrCb video interface)
Pixel Fill Factor	88%
Display Pixel Pitch	5.5um
Display Frame Rate	60 Hz/360Hz (NTSC), 50Hz/300 Hz (PAL)
Data Clock Rate	36 MHz (Typical)
Maximum Brightness	200 cd/m^2 or more
Contrast Ratio	150:1（Typical）
White Point	(x, y)=(0.313, 0.329) Typical
Digital Display Interface	YCbCr(4:2:2)-parallel (16 data, Hd, Vd, Clock)
Control Interface	Industry-standard two-wire bidirectional serial
Operating Supply Voltages	1.8 V (Core) 3.3 V (Analog, I/O) 3.3 V (Analog, LED) VIO_serial (Serial interface I/O)
Iput Signal Level	CMOS 1.8V～3.3V
Power consumption *1	180mW（Reference）
Size（L×W×H）	20.6 x 17.8 x 13.3 (mm)
Weight	TBD
Operating Temperature	-10℃ ~ 70℃ (at Surface of Panel）
Storage Temperature	-30℃ ~ 83℃

*1 Typical value at 60 Hz NTSC (gamma correction of 2.1),
Operation with flat field video pattern(data=FFh) at room temperature under the following values.
VCC=1.80V, VCCX=3.00V, DAVCC=3.30V, VIO_serial=3.30V

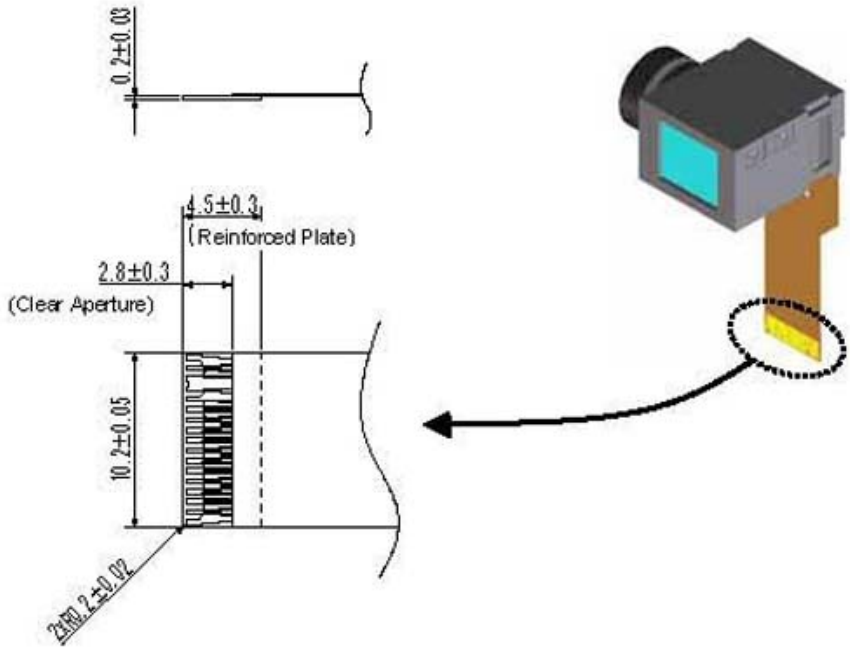
*2 The above sizes of the display format, display panel active area and display area diagonal shows the muximum display size available.
Real VGA(640 x 480) display or other lower resolution setting is also available.
According to the lower display area, a custom aperture is also available.

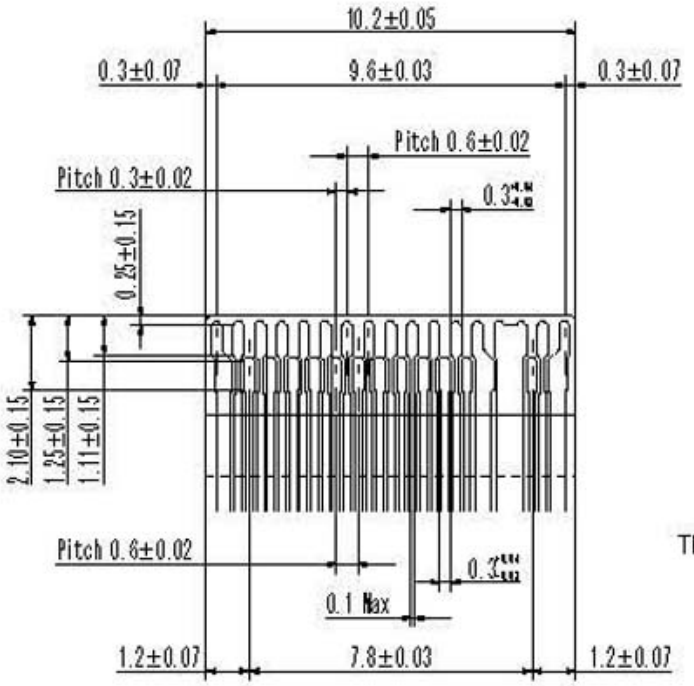
3.Product Appearance

3.1 Appearance Specifications



3.2 Flex Specifications





Terminal Pattern Magnified View

The following is the recommendable connector.
JST Mfg. Co., Ltd.
33FXRH-SM1-GAN-TF(LF)(SN)

Fig1. FPC Terminal Specification

4. Electrical Characteristics

4.1 Degital Video Interface

4.1-1 Video Input Signal Format

The following two kinds of input formats are applicable to this product.

1) YCbCr 4:2:2 Format 16bit Parallel
2) YCbCr 4:2:2 Format 8bit Serial

4.1-2 Video Input Signal Timing

All video input signals must meet the timing requirements shown in the Fig. 2, 3-1, 3-2 & Table 3, 4-1, 4-2, 4-3.

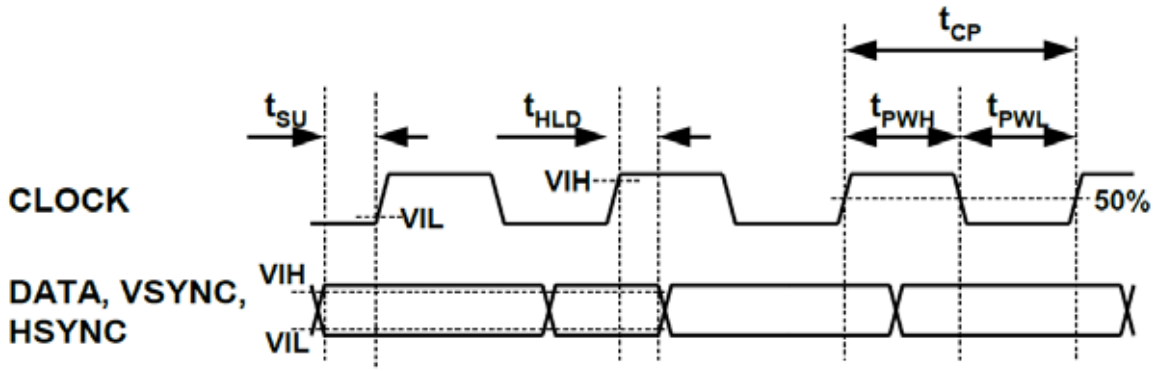


Fig. 2. Video Input Signal Timing

Table 3. AC Characteristics（Video Input Signal Timing）

Parameter	Simbol	Min.	Typ.	Max.	Unit
CLOCK, rate	$1/t_{CP}$	25	36	75	MHz
CLOCK, pulse width high	t_{PWH}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
DATA、VSYNC、HSYNC、setup time	t_{SU}	1.25			ns
DATA、VSYNC、HSYNC、hold time	t_{HLD}	1.25			ns

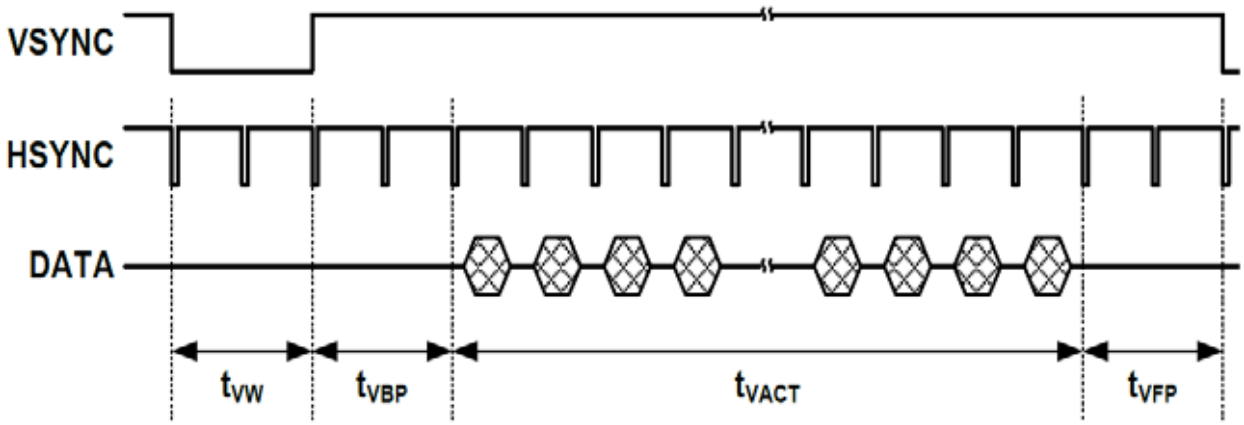


Fig. 3-1. Video Input Vertical Timing

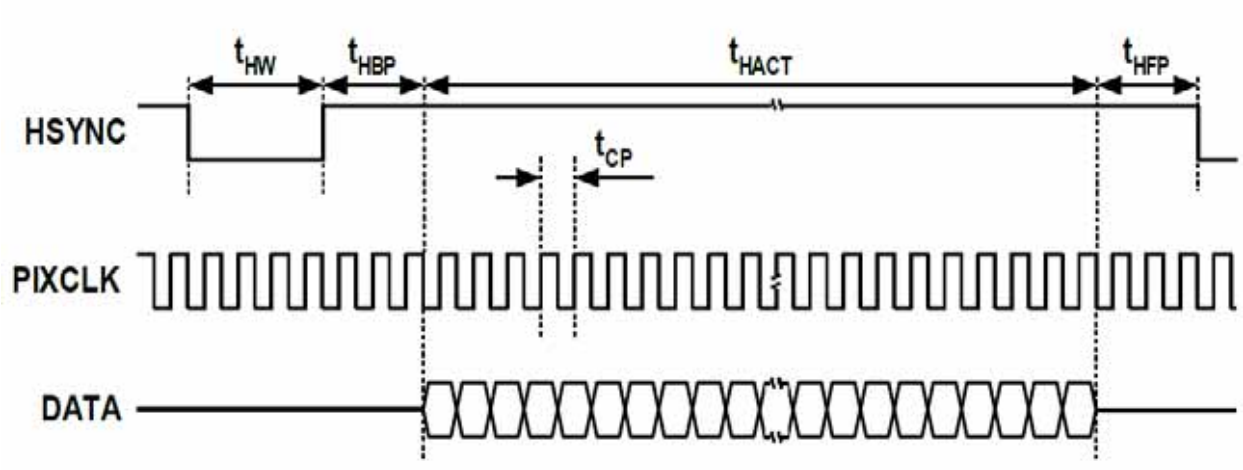


Fig. 3-2. Video Input Horizontal Timing

4.1-3 Video Input Field Detection

In case the number of clock of T-Field shown in the Fig. 3-3 is one-fourth or more and less three-fourths of the total clocks of HSYNC, the field is detected as "Even" field.
In other cases, the field is detected as "Odd" field.

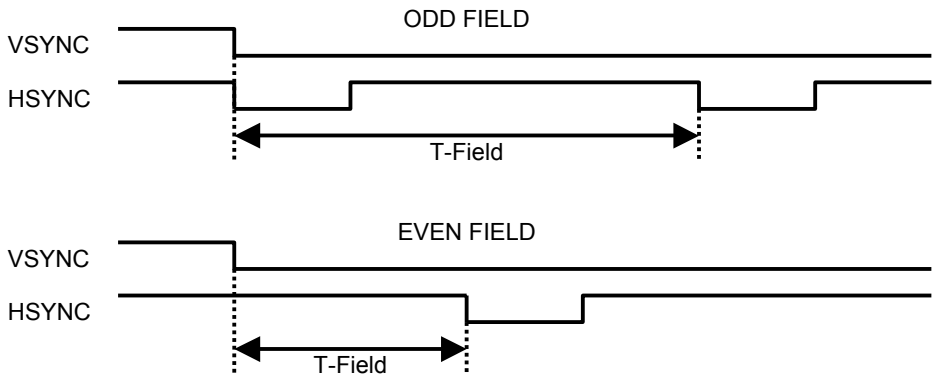


Fig. 3-3. Video Input Field Detection

Table 4-1. Parallel Data AC Characteristcs Video Format Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC, frequency	t_{VF}	47		63	Hz
VSYNC, total lines	t_{VTOT} = $t_{VBLK} + t_{VACT}$	282		1088	Lines
VSYNC, active lines	t_{VACT}	480			Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	12		200	Lines
VSYNC, front porch (*1)	t_{VFP}	5 (*1)		94	Lines
VSYNC, pulse width	t_{VW}	3		94	Lines
VSYNC, back porch	t_{VBP}	3		94	Lines
HSYNC, total clocks	t_{HTOT} = $t_{HBLK} + t_{HACT}$	524		1392	Clocks
HSYNC, active clocks (*2)	t_{HACT}	640			Clocks
HSYNC, blanking	t_{HBLK} = $t_{HFP} + t_{HW} + t_{HBP}$	24		512	Clocks
HSYNC, front porch	t_{HFP}	12		512	Clocks
HSYNC, pulse width	t_{HW}	4		128	Clocks
HSYNC, back porch	t_{HBP}	8		512	Clocks
CLOCK, rate	$1/t_{CP}$	25		75	MHz

*1**:** The minimum VSYNC front porch must be greater than 5,000 clocks.
*2**:** Defalt setting is applicable to VGA(640H X 480V) active data input only.
When other active date input is needed, please contact us.

Table 4-2. Serial Data AC Characteristcs Video Format Timing

Parameter	Simbol	Min.	Typ.	Max.	Unit
VSYNC, frequency	t_{VF}	47		63	Hz
VSYNC, total lines	t_{VTOT} = $t_{VBLK} + t_{VACT}$	492		1088	Lines
VSYNC, active lines	t_{VACT}		480		Lines
VSYNC, blanking	t_{VBLK}= $t_{VFP} + t_{VW} + t_{VBP}$	12		200	Lines
VSYNC, front porch (*1)	t_{VFP}	5 (*1)		94	Lines
VSYNC, pulse width	t_{VW}	3		94	Lines
VSYNC, back porch	t_{VBP}	3		94	Lines
HSYNC, total clocks	t_{HTOT} = $t_{HBLK} + t_{HACT}$	1316		3286	Clocks
HSYNC, active clocks	t_{HACT}		1280		Clocks
HSYNC, blanking	t_{HBLK} = $t_{HFP} + t_{HW} + t_{HBP}$	36		512	Clocks
HSYNC, front porch	t_{HFP}	24		512	Clocks
HSYNC, pulse width	t_{HW}	4		128	Clocks
HSYNC, back porch	t_{HBP}	8		512	Clocks
CLOCK, rate	$1/t_{CP}$	50		76	MHz

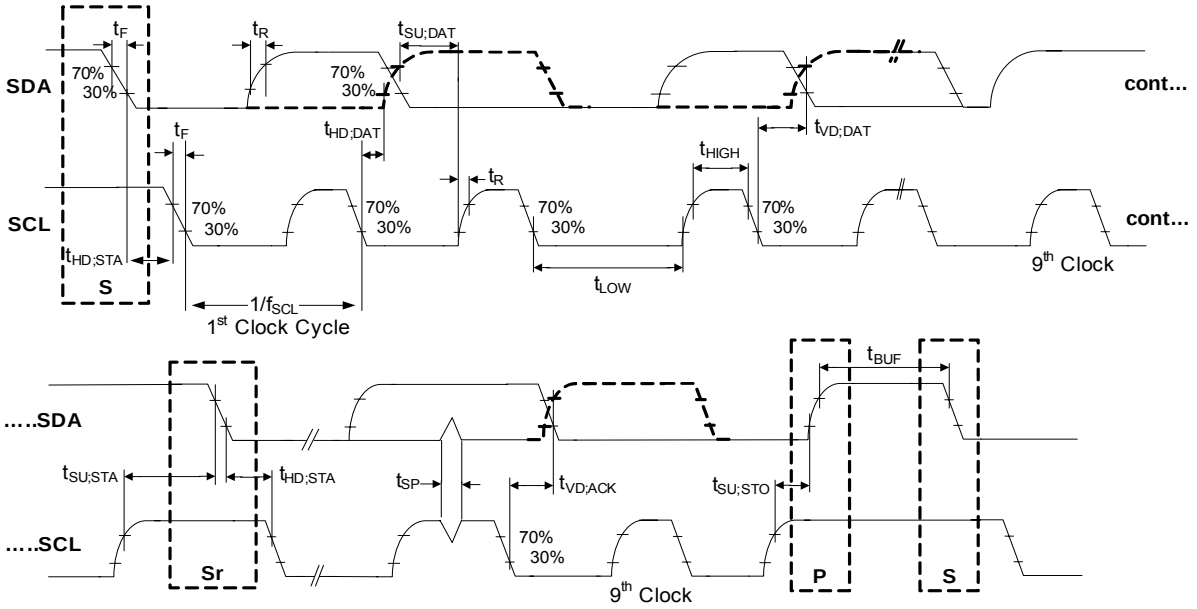
*1: The minimum VSYNC front porch must be greater than 5,000 clocks.

*2: Defalt setting is applicable to VGA(640H X 480V) active data input only.
When other active date input is needed, please contact us.

4.2 Control Interface

4.2-1 AC Characteristics of Interface Signal

This product is controlled by writing data in the control registers with I2C interface.
The AC characteristics of interface signal are as follows.



V_{IH}, V_{IL} Values & Definition **:**
Please refer to [4.5 Rating]

Fig. 5. I2C Interface Signal

Table 5. AC Characteristics（I2C Interface）

Symbol	Parameter	Conditions	Standard-Mode		Fast-Mode		Unit
			Min.	Max.	Min.	Max.	
fSCL	SCL clock frequency		0	100	0	400	KHz
tHD;STA	hold time (& repeated) START condition	After this period, the first clock pulse is generated.	4	-	0.6	-	us
tLOW	LOW period of the SCL clock		4.7	-	1.3	-	us
tHIGH	HIGH period of the SCL clock		4	-	0.6	-	us
tSU;STA	set-up time for a repeated START condition		4.7	-	0.6	-	us
tHD;DAT	data hold time		0	-	0	-	us
tSU;DAT	data set-up time		250	-	100	-	ns
tr	rise time of both SDA and SCL signals		-	1000	20+0.1Cb	300	ns
tf	fall time of both SDA and SCL signals		-	300	20+0.1Cb	300	ns
tSU;STO	set-up time for STOP condition		4	-	0.6	-	us
tBUF	bus free time between STOP and START condition		4.7	-	1.3	-	us
Cb	capacitive load for each bus line (depends on load and frequency)		-	400	-	400	pF
tVD;DAT	data valid time		-	3.45	-	0.9	us

4.2-2 Protcol

This FLC device is always considered a slave in the system and requires a clock to be provided to it for all I2C interface transactions.

Start Condition **:** A start condition is generated through the use of pulling down the SDA line while SCL is still high.

Slave Address **:** 7bit -- 0111110b

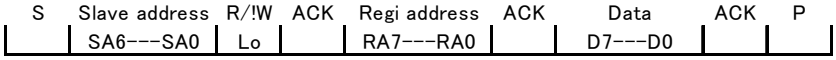
R/!W bit **:** The 8th bit -- If a READ is requested then the bit should be kept high, and if a WRITE is requested, the line is pulled down to a low-level signal.

ACK bit **:** The 9th bit -- the acknowledgment bit from the addressed device.
If the addressed device receives its address and is not busy at that time it will respond by pulling the SDA line low and therefore signaling an acknowledgment. If an acknowledgment is detected by the issuing device, then the rest of the message can be sent.

Stop Condition **:** If SCL is kept high and SDA changes from low to high, the interface stops.

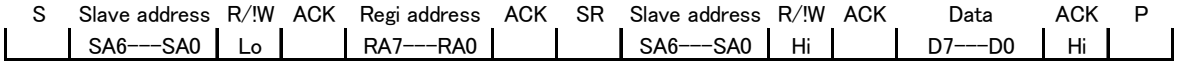
Single Write Protocol

A START signal must be presented first. This is when the SDA line is pulled low while the SCL line is kept high. The first byte sent is always the slave address for the qHD panel's I2C interface (0111 110b) followed by the R/!W bit(Lo). An acknowledge (ACK) is returned from the receiving device after each byte sent by pulling the SDA line low for one clock. The clock is still provided by the master device, which is never the qHD panel display. The second byte sent in the write transactions is the qHD panel's 8-bit register address that will be written. After the register address is sent, the byte to be written is sent. The master keeps control of the bus and delivers the byte to be written.



Single Read Protocol

After a START, the slave address and R/!W(Lo) are sent. After an ACK is returned from the receiving device, the register address to be read is sent. Again after an ACK is returned from the receiving device, a START signal is presented again and the slave address is sent followed by the R/!W bit(Hi). After an ACK is returned, the device reads the byte data but not return an ACK. Then, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.



* SR : Restart

Multi-Write Protocol

Similar to single write protocol, after transactions of a START, the slave address, R/W!(Lo), an ACK, and byte data in that order, by continuously outputting data, the register address is auto-incremented for each byte write. After all data are written in the necessary addresses, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.

Multi-Read Protocol

Similar to single read protocol, after transactions of a START, the slave address, R/W!(Lo), an ACK, the register address, a START(SR), the slave address, R/!W(Hi) and an ACK in that order, by continuously reading data, the register address in the device is auto-incremented and the data is output. After all data are read in the necessary addresses, not returning an ACK, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.

4.3 Control Sequence Requirements

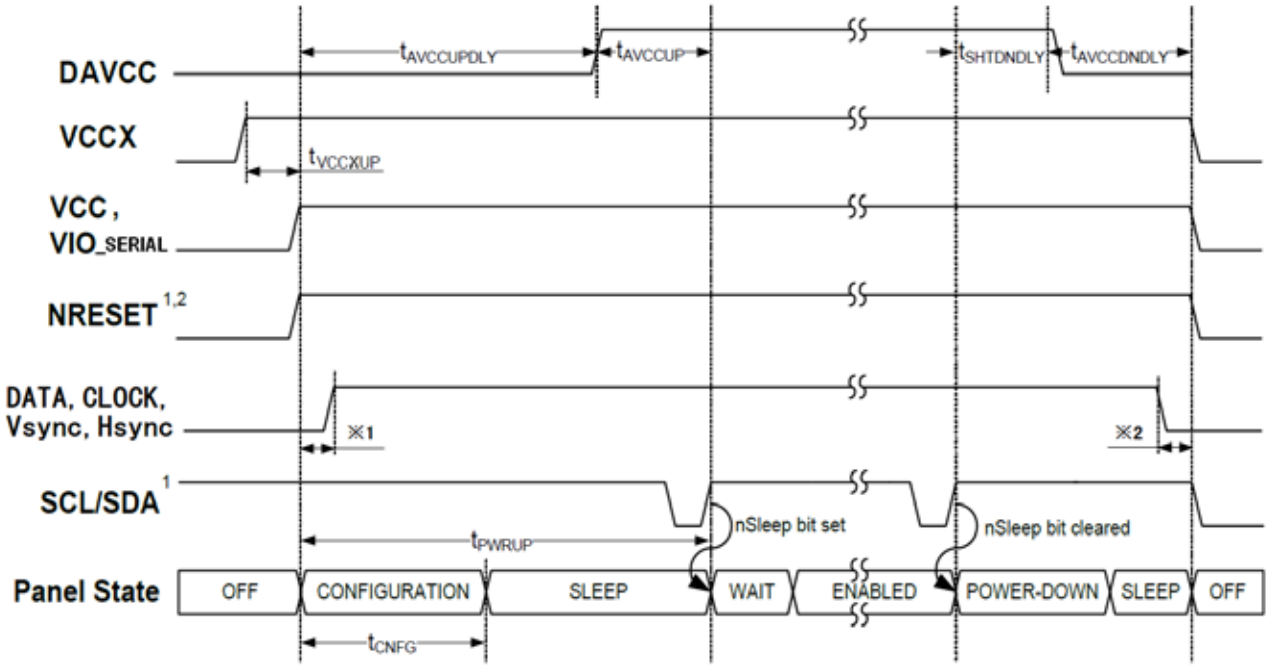
Timing/sequence requirements must be met during start-up and shut-down of the display panel to avoid damages to the display panel.

4.3-1 Start-up Sequence Requirements

The VCCX power supply must be present before the VCC power suppy is present.
After the VCCX power supply is present, the VCC, VIO_serial must be present for a time period of tVCCXUP.
After the voltage supplies (VCC, VIO_serial) are present and in specification, the NRESET input is high and the CLOCK input is toggling, the display panel will load default register values from non-volatile memory to RAM for a time period of tCNFG. During this time period, the two-wire serial interface is ignored.
Although the voltage supplies (VCC, VCCX, VIO_serial) can be present simultaneously, the tCNFG starts when the VCC power supply is in specification and the NRESET input is high.
(* As the NRESET is pulled up, the NRESET becomes high even on an open state when the VCC power supply is present.)
After the tCNFG period, the display panel will be in the Sleep mode and the two-wire serial interface is active.
After a time period of tPWRUP(The tPWRUP starts when the VCC power supply is in specification and the NRESET is high.), the nSleep bit can be cleared by using the serial interface.
The voltage supplies (VCC, VCCX, VIO_serial) must be present for a time period of tAVCCUPDLY before the DAVCC power supply is present. A minimum time period of tAVCCUP exists which is time from when the DAVCC supply is present till when the nSleep bit can be cleared. If a valid video signal is not present or the nSleep bit is not cleared, the display panel keeps the Sleep mode and no image is driven.
The video signal（DATA0～15,CLOCK,Vsync,Hsync）must be present at the time when or after all the voltage supplies (VCC,VCCX,VIO_serial) are present as shown in Figure 6. When a video signal is detected and the nSleep bit is cleared, a voltage is supplied to the liquid crystal in the display and images are driven.

4.3-2 Shut-down Sequence

In case of shut-down of the display, an operationg voltage to the liquid crystal must be shut by putting the display panel into sleep mode before the voltage supplies are stopped.
After nSleep bit is set through the serial interface, each power supply including the DAVCC and the NRESET must be kept high for a time period of tSHTDNDLY. After that, the DAVCC power supply is stopped first and, after a time period of tAVCCDNDLY, the voltage supplies (VCC, VCCX, VIO_serial) must be stopped. However, the video signals(DATA0～15,CLOCK,Vsync,Hsync）must be stopped before the voltage supplies (VCC, VCCX, VIO_serial) are stopped as shown ※2 in Figure 6.



[1] NRESET and SCL/SDA are relative to the VCC supply.
[2] NRESET may be left unconnected in the display system.

Fig. 6. Start-up/Shut-down Sequence

Table 6. AC Characteristics (Control Sequence Timing)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Time from VCCX supply to VCC,VIO_serial supply	t_{VCCXUP}	0	-	5	ms
Time from VCC supply and NRESET Hi till when Configuration is finished.	t_{CNFG}	23	-	40	ms
Time from VCC supply and NRESET Hi till when nSleep bit can be cleared through serial interface.	t_{PWRUP}	40	-	-	ms
Time from VCCX,VCC,VIO_serial supply till when DAVCC can be supplied.	$t_{AVCCUPDLY}$	400	-	-	us
Time from DAVCC supply till when nSleep bit can be cleared through serial interface.	t_{AVCCUP}	1	-	-	ms
Time from when nSleep bit is set through serial interface till when DAVCC supply can be stopped.	$t_{SHTDNDLY}$	1	-	-	ms
Time from when DAVCC supply is stopped till when VCCX,VCC,VIO_serial supplies can be stopped.	$t_{AVCCDNDLY}$	40	-	-	ms

4.3-3 Sleep Mode

During a Sleep mode, the diplay holds each register value, and when a Sleep mode is cleared, the display becomes an ordinal operation mode. During a Slep mode, the serial interface is available and reading & writing are available without any input of clock.

4.3-4 Complementary Precaution Statements

* When each register is written with a certain value, the value reflects the operation of the display.

* To prevent the display image from being distorted or other failure, the nSleep bit must be cleared while a video signal (DATA0～15,CLOCK,Vsync,Hsync) is present.

* if the nSleep bit is cleared during a period other than the time from the Vsync to {the value set in the vvld_delay register(0Ch) - 2}line, the vertical position of the image primarily displayed may be shifted from the proper position.

4.4 Pin Assignments

Table 7. Pin Assignments

No	Name	I/O	Power Supply	Function	
				16bit Parallel	8bit Serial
1,2	GND	NA	NA	Ground	
3	DATA 15	I	1.8V ~ 3.3V	Cb7/Cr7	GND
4	DATA 14	I	1.8V ~ 3.3V	Cb6/Cr6	GND
5	DATA 13	I	1.8V ~ 3.3V	Cb5/Cr5	GND
6	DATA 12	I	1.8V ~ 3.3V	Cb4/Cr4	GND
7	DATA 11	I	1.8V ~ 3.3V	Cb3/Cr3	GND
8	DATA 10	I	1.8V ~ 3.3V	Cb2/Cr2	GND
9	DATA 9	I	1.8V ~ 3.3V	Cb1/Cr1	GND
10	DATA 8	I	1.8V ~ 3.3V	Cb0/Cr0	GND
11	DATA 7	I	1.8V ~ 3.3V	Y7	Y7/Cb7/Cr7
12	DATA 6	I	1.8V ~ 3.3V	Y6	Y6/Cb6/Cr6
13	DATA 5	I	1.8V ~ 3.3V	Y5	Y5/Cb5/Cr5
14	DATA 4	I	1.8V ~ 3.3V	Y4	Y4/Cb4/Cr4
15	DATA 3	I	1.8V ~ 3.3V	Y3	Y3/Cb3/Cr3
16	DATA 2	I	1.8V ~ 3.3V	Y2	Y2/Cb2/Cr2
17	DATA 1	I	1.8V ~ 3.3V	Y1	Y1/Cb1/Cr1
18	DATA 0	I	1.8V ~ 3.3V	Y0	Y0/Cb0/Cr0
19	HSYNC	I	1.8V ~ 3.3V	Horizontal Synch Signal	
20	GND	NA	NA	Ground	
21	VYSNC	I	1.8V ~ 3.3V	Vertical Synch Signal	
22	VIO_Serial	NA	NA	I/O voltage supply for serial interface pins	
23	SCL	I	VIO_Serial	Serial Interface Clock Input	
24	SDA	IO	VIO_Serial	Serial Interface Data I/O	
25,26	DAVCC	NA	NA	LED Driver Power Supply（+3.3V）	
27,28,29	VCC(*3)	NA	NA	Panel Core Power Supply（+1.8V）	
30	VCCX	NA	NA	Panel / EEPROM Power Supply（+3.3V）	
31	CLOCK	I	1.8V ~ 3.3V	Video Data Clock	
32,33	GND	NA	NA	Ground	

*1: A mapping of video data signal for DATA0~15 can be changed.
The details are referred to in [5.Configuration Register Settings] .

*2: It is recommendable to put a 10uF or larger decoupling capacitor to the VCC on a operation circuit side.

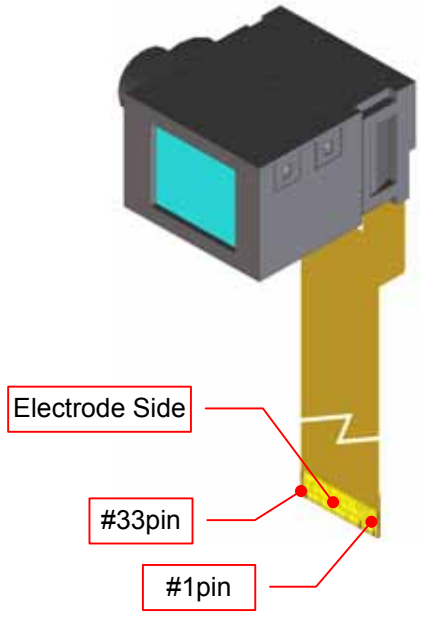


Fig. 7. Pin Location

4.5 Ratings

Table 8. Absolute Maximum Ratings

Parameter	Absolute Maximum Rating		Unit
	Min.	Max.	
VCCX	-0.5	3.6	V
VCC	-0.5	1.95	V
DAVCC	-0.5	3.6	V
V_{IO_Serial}	-0.5	3.6	V
Voltage on any Video Input Pin	-0.4	VCCX + 0.4	V
Voltage on any Serial Input Pin	-0.4	$VIO_{\_Serial}$+0.4	V

Table 9. DC Characteristics

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	VCCX	*1	2.9	3.0	3.1	V
	VCC	*1	1.8	1.8	1.95	
	DAVCC	*1	3.0	3.3	3.6	
	VIO_serial	*1	1.65	3.3	3.6	
*1: While operating, the VCCX and VCC must fulfill the above conditions.						
Input Voltage	VIH	For all video inputs	0.8*VCC			V
		For all serial inputs	0.8*VIO_serial			
	VIL	For all video inputs			0.18*VCC	
		For all serial inputs			0.18*VIO_serial	
Input Capacitance	IC	For all inputs 3.3Vp-p, f=5MHz		6	12	pF
Input Leakage Current	IIL	VI = VIL	-10			uA
	IIH	VI = VIH			10	
Average panel operating supply current <Measurement Conditions> VCC=1.80V, VCCX=3.30V, DAVCC=3.30V, VIO_serial=3.30V, Input Resolution=640x480 (16bit parallel), Display Resolution=720*540 (Scaling Up), Image = White Raster CLOCK =40MHz, Field Frequency=60Hz	I_{VCCX}	Nomal Mode		4.8	6	mA
		Sleep Mode		2.1	3	
	I_{VCC}	Nomal Mode		80	86	
		Sleep Mode		1.8	5	
	I_{DAVCC}	Nomal Mode		6	12	
		Sleep Mode		3	5	
	IVIO_serial	Normal Mode		0.1	0.5	
		Sleep Mode		0.1	0.5	

4.6 Electronic Circuit Diagram

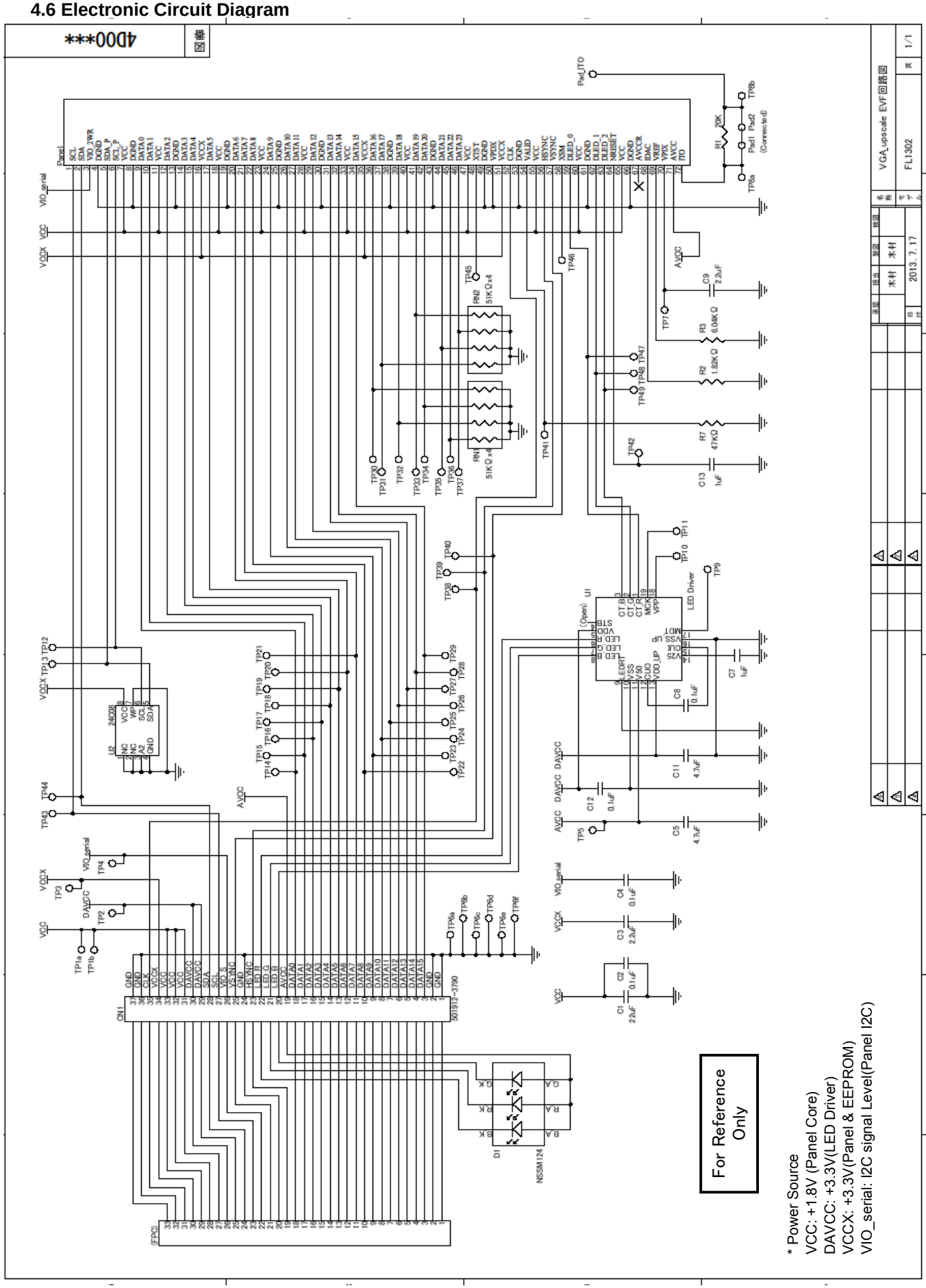


Fig.8. Electronic Circuit Diagram

5. Configuration Register Settings

Register Index : 00h

Bit	7	6	5	4	3	2	1	0
Meaning	dither_mode[3:0]				Res			
Value(e.g.)	0000				0000			

Dither_Mode: Select dither mode
4'h1=1/2bit Spatial Dither , 1/4bit Temporal Dither
4'h2=1/2bit Temporal Dither, 1/4bit Spatial Dither
4'h3=1/2bit Spatial Dither
4'h5=Reserved（Not Available）
4'h6=Reserved（Not Available）
other= No Dither / Input data rounded to 7-bit values

Res: Reserved
The data of all "Res" register must be 0h for the proper operation.

Register Index : 01h

Bit	7	6	5	4	3	2	1	0
Meaning	cspace_sel	channel_map[2:0]			data_channel[1:0]		data_seq[1:0]	
Value(e.g.)	1	000			01		00	

cspace_sel: Color Space Select
the data must be "1" for this display panel.

channel_map: select mapping of data channel to color information, dependent on the data channel setting according to the following table.

channel_map	16-bit YCbCr		8-bit YCbCr	
	[15:8]	[7:0]	[15:8]	[7:0]
0h	Cb/Cr	Y		Y/Cb/Cr
1h	Y	Cb/Cr	Y/Cb/Cr	
2h～7h	Reserved（Not Available）			

data_channel: select data interface
01=16bit data interface
10=8bit data interface
other=Reserved（Not Available）

data_seq: data sequence of color information for 8-bit and 16-bit interfaces.

DataSequence	16-bit YCbCr	8-bit YCbCr
00	Reserved（Not Available）	[Cb][Y_0][Cr][Y_1]
01	[Y_0Cr] [Y_1Cb]	[Cr][Y_0][Cb][Y_1]
10	Reserved（Not Available）	[Y_0][Cb][Y_1][Cr]
11	Reserved（Not available）	[Y_0][Cr][Y_1][Cb]

6.Display Panel Specification

6.1 Optical Characteristics

Table 10. Optical Characteristics（at Room Temp.）

Item	Conditions		Min.	Typ.	Max.	Unit
Brightness	White Raster Image Measure the brightness of the center of the display.		200	220		cd/m^2
Contrast Ratio	White Raster ／Black Raster Image Measure the brightness ratio of the center of the panel.		100:1	150:1		-
xy Chromaticity	White Raster Image Measure the chromaticity of the center of the panel.	x	0.303	0.313	0.323	-
		y	0.319	0.329	0.339	-

Note **:** Measurement conditions of the optical characteristics are as follows.

[Measurement Conditions]

Supply Voltage : VCC=1.80V, VCCX=3.30V, VIO_serial=3.30V, DAVCC=3.30V
Video Signal Input : YCbCr 16bit
White Y=FFh, Cb=80h, Cr=80h
Gamma Correction : 2.1
LED brightness register : Setting at maximum

Temperature : Room Temp.（25℃ Typ.）
Luminance & Color Mete : CS-100A manufactured by Konica minolta
xy Chromaticity : Measured on white image
Brightness : Measured on white image

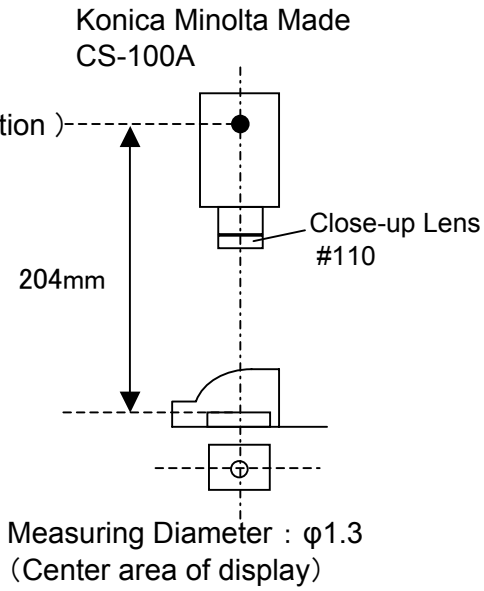


Fig.12. Optical Measurement

6.2 Lens Optical Characteristics (Design value）

Table15. Lens Optical Characteristics

Parameter	Standard value	Unit	Remarks
Magnification of ocular	18.4	times	（250/f）
Focal length	13.59	mm	
Diameter of exit pupil	φ5.0	mm	
Eye Point	12.5	mm	From the eye side lens top to the viewpoint.(0d)
Adjustment range of the diopter	-3 ~ +1	D	
Wavelength range	440～650	nm	
Lens constitution	3	pcs	
MTF (Modulation transfer function)	Center **:** 94.1% / 40lp/mm V (Y=1.485)**:** M 71% / 40lp/mm S 67% / 40lp/mm H (Y=1.98)**:** M 62% / 40lp/mm S 39% / 40lp/mm		
Peripheral brightness	91.9	%	
DISTORTION	-0.54	%	Optics Distortion (Diagonal)
	-0.13	%	TV Distortion
Chromatic aberration of magnification	0.0057	mm	Diagonal, the distance between C line and g line.
	0.0038	mm	Diagonal, the distance between d line and F line.
Coating	No Coating		

*1 : All values are at room temperature, under the general environment.
*2 : All values are theoretically calculated by CFM.

6.3 Visual Specifications

Conditions of inspection

At room temperature and normal humidity, inspect the display by microscope of 20 magnification focusing on the display focal plane.

Dither mode setting **:** 1/2bit spatial dither & 1/4bit temporal dither Gamma correction setting **:** 2.1

Color space/ Color offset register setting **:** 0h(All setting)

Input Signal Level 0%**:** (Y,Cb,Cr)=(0h,80h,80h), 100%**:** (Y,Cb,Cr)=(FFh,80h,80h)

Table 16-1. Display area visual defects

Subject Area	Item	Size（Average）[Unit **:** μm^2]	Allowable Quantity[Unit: pcs]	
			Bright/White spot Scratch（White）	Dark/Black point Scratch(Black)
Display area Dummy area Aperture mask	Line Out	1 pixel line(line/column	0	0
	Large Spot	S > 121	0	0
	Medium Spot	121 ≥ S > 61	3	3
	Small Spot	61 ≥ S	No clumping	
Display area	Texture	According to limit sample		
PBS Upper side/ Lower side	Contamination Scratch	None when focusing on the display focal plane		

Note 1）Definition of display area is shown in Figure 13.

Note 2）Contaminations and scratches with line shape are judged after converting the size into area.

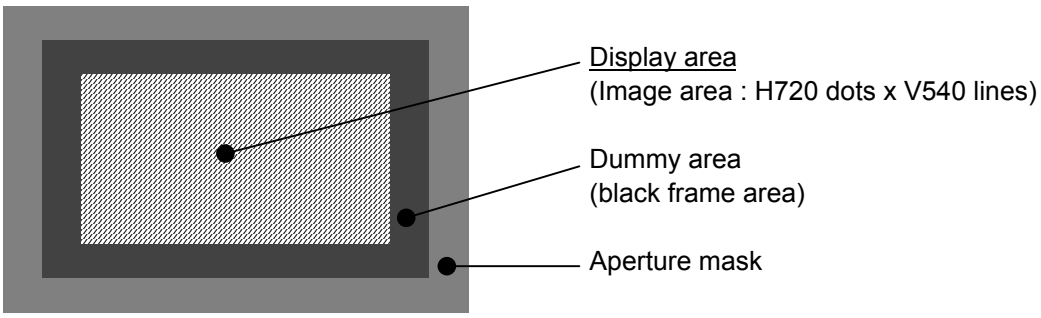


Fig. 13. Display area

[Appearance and Mechanical feature]

Table16-2.Appearance and Mechanical feature

Item (a-d: Refer to Fig.14)		Spec.	Measuring condition / Note
a b c	Scratch Burr Contamination	Should not degrade appearance quality. (*1)	With naked eyes.
d	Contamination Scratch Trash	Should not degrade appearance quality. (*1)	*2
Lens	Contamination Scratch Trash	Should not degrade appearance quality. (*1)	*2
	Blur	Should not degrade appearance quality. (*1)	Focusing on the displayed image.
Dial movement	Rotary torque	**TBD** to **TBD** cNm	
	Operational feeling	Should move smoothly. No excess backlash and rattling.	

*1 : Limit samples are to apply to the criteria for judgement, if necessary.
*2 : Focusing on the displayed image. Additionally inspect with a white image keeping an eye away from the eyepiece lens.

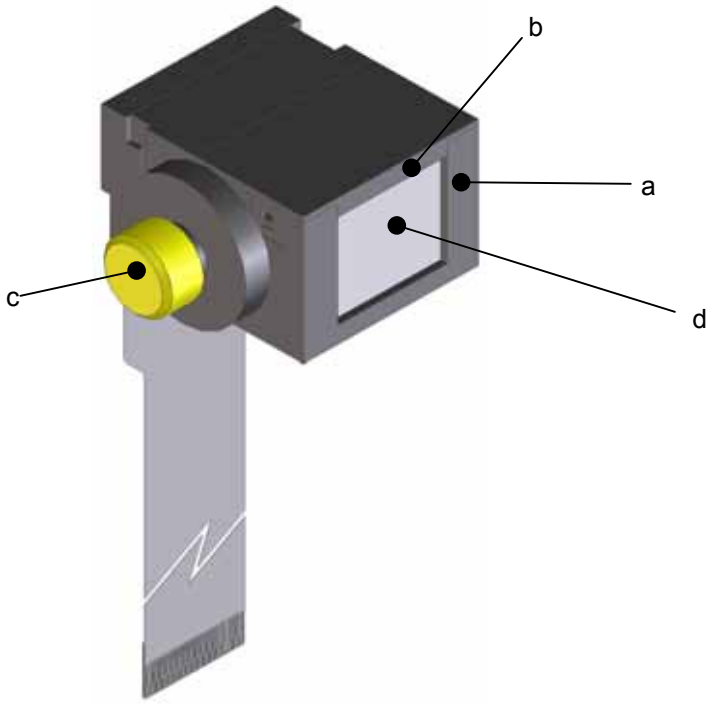


Fig14: Inspection point designation

7.Serial Number

1) Serial No

X	X	XXXXXX	X
a	b	c	d

a : Manufacturing Year -- Last digit of the western calendar year

b : Manufacturing Month -- shown by 1 digit as below

Jan. ...	A	Jul. ...	G
Feb. ...	B	Aug. ...	H
Mar. ...	C	Sep. ...	I
Apr. ...	D	Oct. ...	J
May ...	E	Nov. ...	K
Jun. ...	F	Dec. ...	L

c : Serial No.（Maximum 6 digits）

d : Model Identification

FLxxxx … TBD

2）Label Color

TBD

3）Labeling Position : Refer to the following figure.

9. Reliability

9.1 Reliability Test

Item	Test Condition	Spec.
High Temperature Storage Test	Ta=83°C 240hrs * Ta : Ambient temperature of this product	Judgement is performed after an hour storage at room temp. Should not have any mechanical and electrical malfunction of product that affects normal product operation.
Low Temperature Storage Test	Ta= -30°C 240hrs	
High Temperature High Humidity Storage Test	Ta=60°C RH=90% 240hrs	
High Temperature Operating Test	Tp=70°C 240hrs * Tp: Surface temperature of panel glass	
Low Temperature Operating Test	Ta= - 10°C 240hrs	
High Temperature High Humidity Operating Test	Ta=40°C RH=90% 240H	
Heat Shock Cycle Test	-30 ~ 80°C 30min/30min 30 cycles	

* Ta : Ambient temperature of the product

9.2 Electrostatic Discharge Test

Item	Test Condition	Spec.
Electrostatic discharge test Mechine Model	C=200PF R=0Ω V=+/- 200V Discharge between Power supply terminal and each signal pin 3 times each.	Should not have any mechanical and electrical malfunction of product that affects normal product operation.

Note : The above tests are performed at room temperature and normal environment.

9.3 Mechanical Reliability Test

Item	Test Condition	Spec.
Vibration Test	Vibration amplitude **:** 1.5mm Frequency **:** 10-55Hz Duration time **:** each axis 30min(X, Y, Z)	Should not have any mechanical and electrical malfunction of product that affects normal product operation.
Drop Test	Height **:** 20cm Drop time **:** each axis 3 times(X, Y, Z) Let products drop to a hard wooden board or a concrete floor.	

Note : The above tests are performed at room temperature and normal environment.

9.4 Shipping Package Test

Item	Test Condition	Spec.
Vibration Test(in package)	Acceleration : 19.6m/s^2 Frequency : 10-50-10Hz Duration time : each axis 30min(X, Y, Z)	Should not have any mechanical and electrical malfunction of product that affects normal product operation.
Drop Test(in package)	Drop Height : 75cm 1corner 3 edges 6 planes Drop time : each axis 1 time(3edges/6planes) Let products drop to a hard wooden board or a concrete floor.	

Note : The above tests are performed at room temperature and normal environment.

10. Special Handling Criteria

* To prevent dust and particulate contamination, It is recommended to open the seal on these trays in a Class 10,000(or better) or equivalent room for incoming inspection or manufacturing integration.

* Do not stack trays higher than **TBD**, or place other heavy material on the trays to prevent damage to the sensitive optical components on the display.

* Do not touch the surface of the polarizing film with bare fingers.
  When removing particulate contaminations on the film, wipe carefully the particulate contaminations off the film with alcohol-soaked soft cloth or cotton swab without any damage to the film.

* Do not use air blow to remove particulate contaminations.
  In case of strong air blow cleaning very close to the product, particles may intrude into the product.

* During either integration or storage, do not allow any moisture or solvent to contact the polarizing film and do not allow condensation to form on the product.

* When handling the product, please pay attention to keep the product static-free and non-chargeable, especially, do not touch the conductive work surface of the product.

11. Environmental Standards

* The product is compliant with RoHS Directive[EUROPEAN DIRECTIVES 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electoronic equipment].

12.Others

When the issue that is not described in this document arises, the both parties will mutually solve it.