

This specification is tentative and subject to change.

# Customer Product Specification

■ Customer

Product Name : Quad-VGA FLCOS EVF Module

Product Number : \_\_\_\_\_

■ Shenzhen Sonicom electronics technology Co.,Ltd.  
Quad-VGA(1280 x 960) EVF Module

Product Name : \_\_\_\_\_

Product Number : SON-FL09

(Receipt Column)

Date :

\*Please return one signed original.

GA Ybn\ Yb`Gcb]Wc` Y`YWfcb]Wg`hW bc`c[ m7 c`z@X"

Longgang TOWN ShenZhen

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Operating Officer :

Verify : \_\_\_\_\_

Verify : \_\_\_\_\_

Verify : - \_\_\_\_\_

\_\_\_\_\_

Person in  
Charge :

\_\_\_\_\_

Sales :

\_\_\_\_\_



## 1. Scope

This specification covers the Electrical Viewfinder with a full color Ferroelectric Liquid Crystal (FLC) display module to be delivered from Shenzhen Sonicom electronics technology Co.,Ltd.

## 2. Specification summary

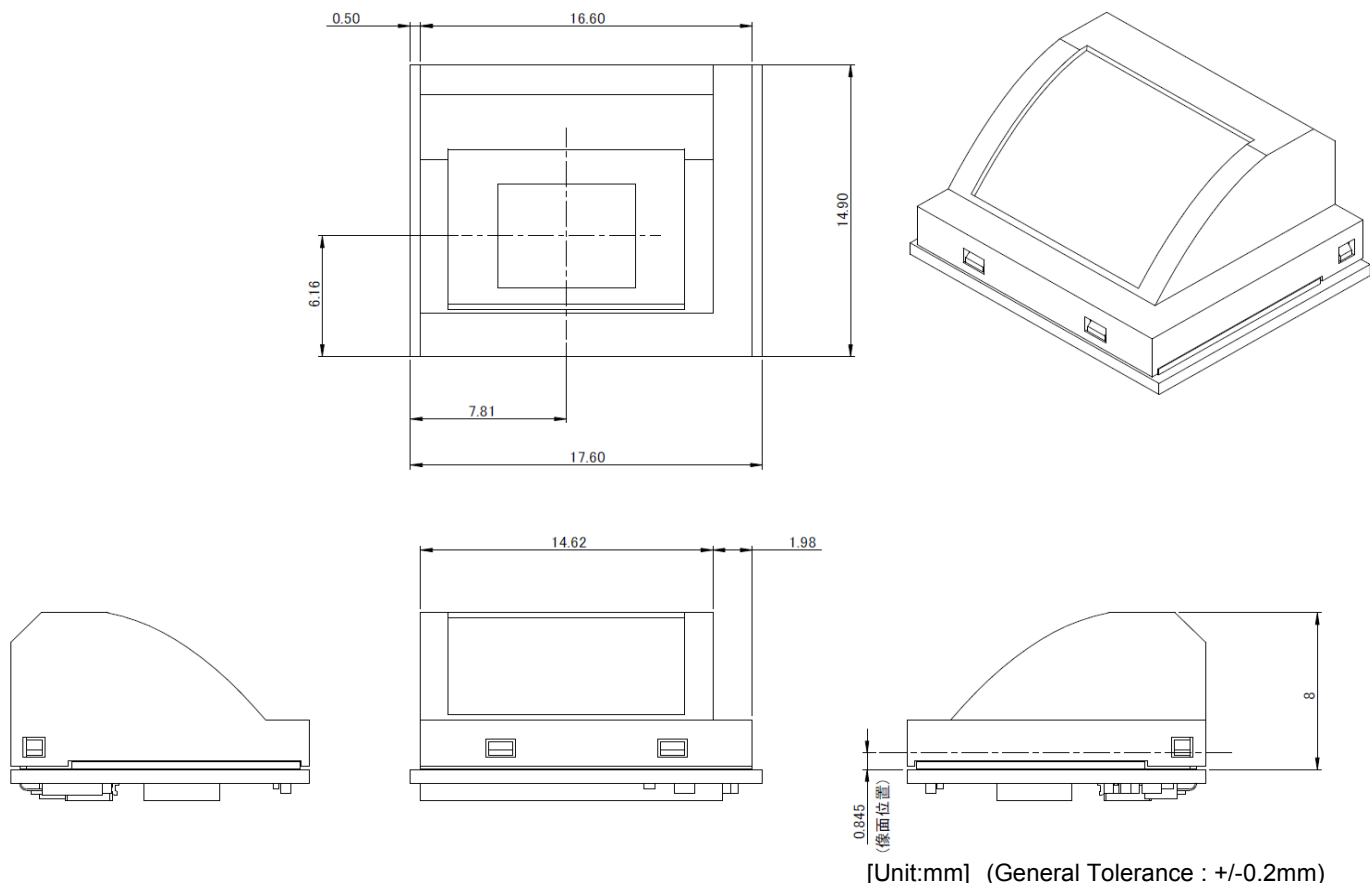
**Table1: Specification summary**

Parameter	Specifications
Display Technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
Display Mode	Field sequential color
Display Format	Quad-VGA : 1,280(H) x 960(V)
Display Panel Active Area	8.127 x 6.095mm
Display Area diagonal	10.16mm (0.40")
Input Grayscale	256 levels per color (8bits)
Color Depth	16.78Million unique colors (RGB 8:8:8 input)
Display Pixel Pitch	6.35um
Display Frame Rate	60 Hz/540Hz (NTSC), 50 Hz/450 Hz (PAL) Typical
Data Clock Rate	25MHz ~ 103MHz
Maximum Luminance	210 cd/m <sup>2</sup> (Typical)
Contrast Ratio	TBD
White Point	(x,y)=(0.312,0.329) (Typical)
Digital Display Interface	RGB888 - parallel 24bit DATA RGB666 - parallel 18bit DATA RGB565 - parallel 16bit DATA YCbCr(4:4:4)-parallel (24 data, Hd, Vd, Clock) YCbCr(4:2:2)-parallel (16 data, Hd, Vd, Clock)
Control Interface	Industry-standard two-wire bidirectional serial
Operating Supply Voltages	1.8 V (Core) 3.3 V (Core) 3.3 V (Analog, LED drive) VIO_serial (Serial interface I/O; 1.8~3.3V)
Input Signal Level	CMOS 1.8V
Power consumption *1	Approx. 360mW (Typical)
Size (L×W×H)	17.6 x 14.9 x 9.7 (mm)
Weight	Approx. 1.7g
Operating Temperature	TBD
Storage Temperature	-30°C ~ 83°C

\*1 Typical value at 60 Hz NTSC (gamma correction of 2.1),  
CCIR-601 operation with flat field video pattern(data= FFh) at room temperature.

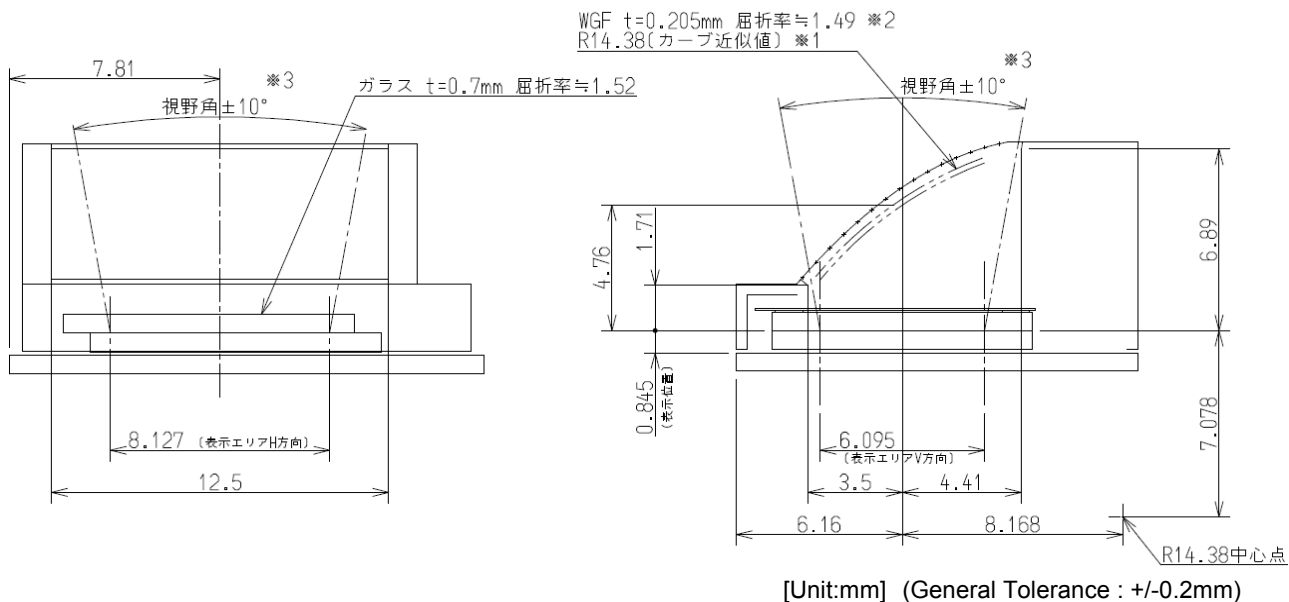
### 3.Product Appearance

#### 3.1 Appearance Specifications



[Unit:mm] (General Tolerance : +/-0.2mm)

**Fig.1-1: Appearance Specifications**



[Unit:mm] (General Tolerance : +/-0.2mm)

- \*1 The cross-section curve of the WGF(Wire Grid Film) is not true circle and is confidential. Please refer to the proximate radius of the curve as R14.38.
- \*2 The WGF consists of a multi-layered structure having any specific refraction index as whole film. As the main material is TAC, please refer to the refraction index of TAC(Approx. 1.49)
- \*3 The View angle is designed center value and not guaranteed value.

**Fig.1-2: Cross-Section View (For optical design purpose)**

## 4. Electrical Characteristics

### 4.1 Digital Video Interface

#### 4.1-1 Video Input Signal Format

The following three kinds of input formats are applicable to this product.

- 1) RGB888 Format 24bit Parallel
- 2) RGB666 Format 18bit Parallel (When using, please contact us for the pin assignment.)
- 3) RGB565 Format 16bit Parallel (When using, please contact us for the pin assignment.)
- 4) YCbCr 4:4:4 Format 24bit Parallel
- 5) YCbCr 4:2:2 Format 16bit Parallel

#### 4.1-2 Video Input Signal Timing

All video input signals must meet the timing requirements shown in the Fig. 2, 3-1, 3-2, 3-3 & Table 2, 3.

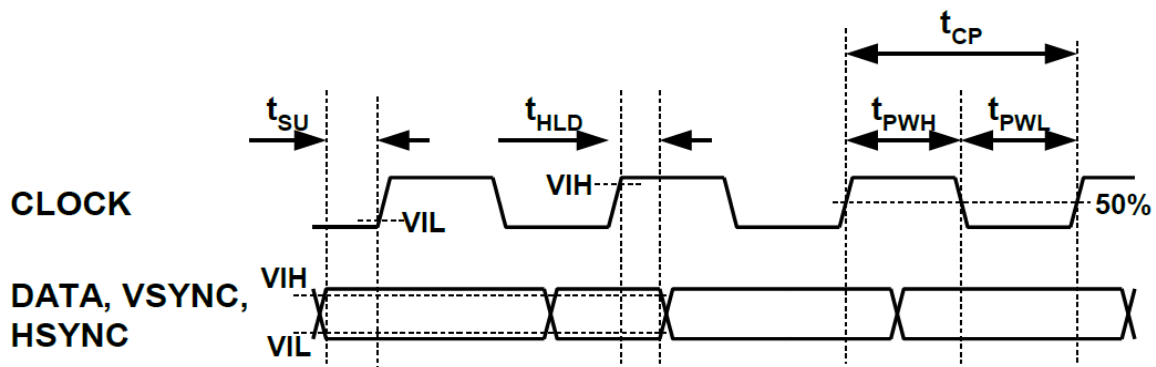


Fig. 2. Video Input Signal Timing

Table 2. AC Characteristics (Video Input Signal Timing)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLOCK, rate	$1/t_{CP}$	25		103	MHz
CLOCK, pulse width high	$t_{PWH}$	40% $t_{CP}$	50% $t_{CP}$	60% $t_{CP}$	NA
CLOCK, pulse width low	$t_{PWL}$	40% $t_{CP}$	50% $t_{CP}$	60% $t_{CP}$	NA
DATA, VSYNC, HSYNC, setup time	$t_{SU}$	1.25			ns
DATA, VSYNC, HSYNC, hold time	$t_{HLD}$	1.25			ns

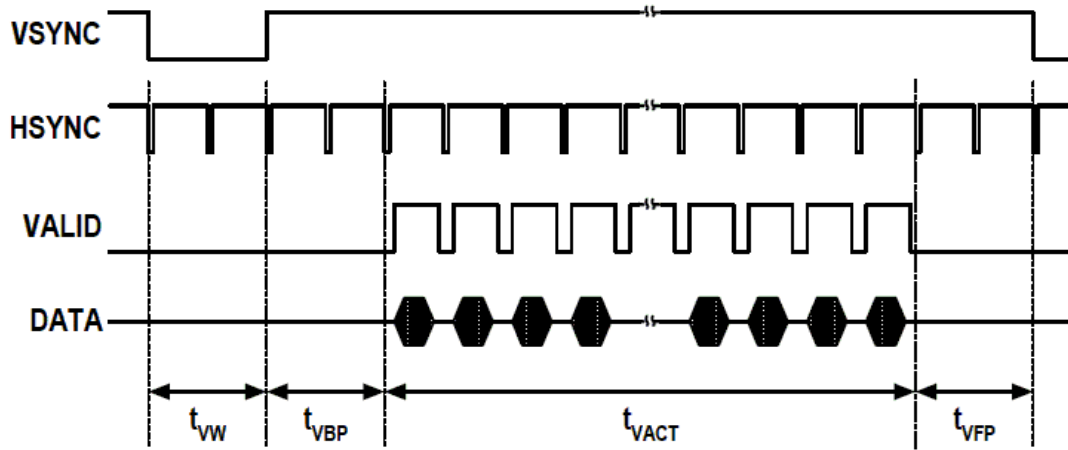


Fig. 3-1. Video Input Vertical Timing

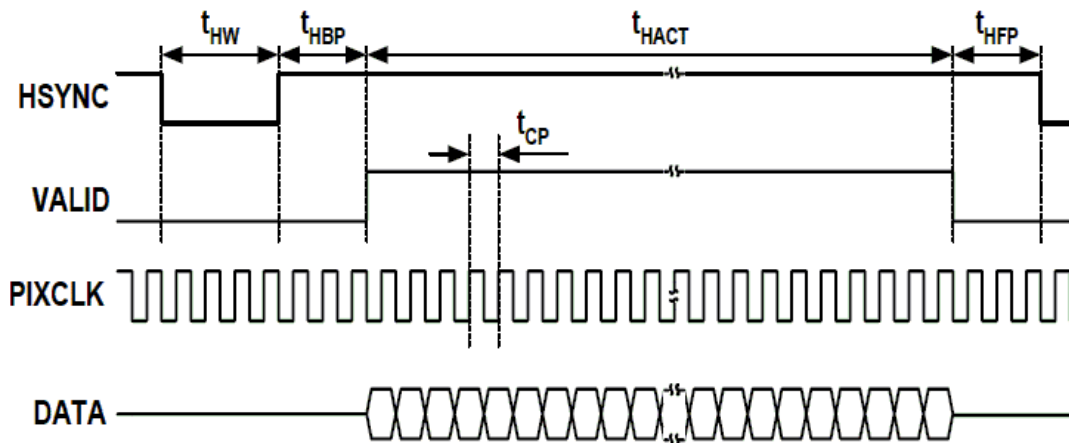


Fig. 3-2. Video Input Horizontal Timing

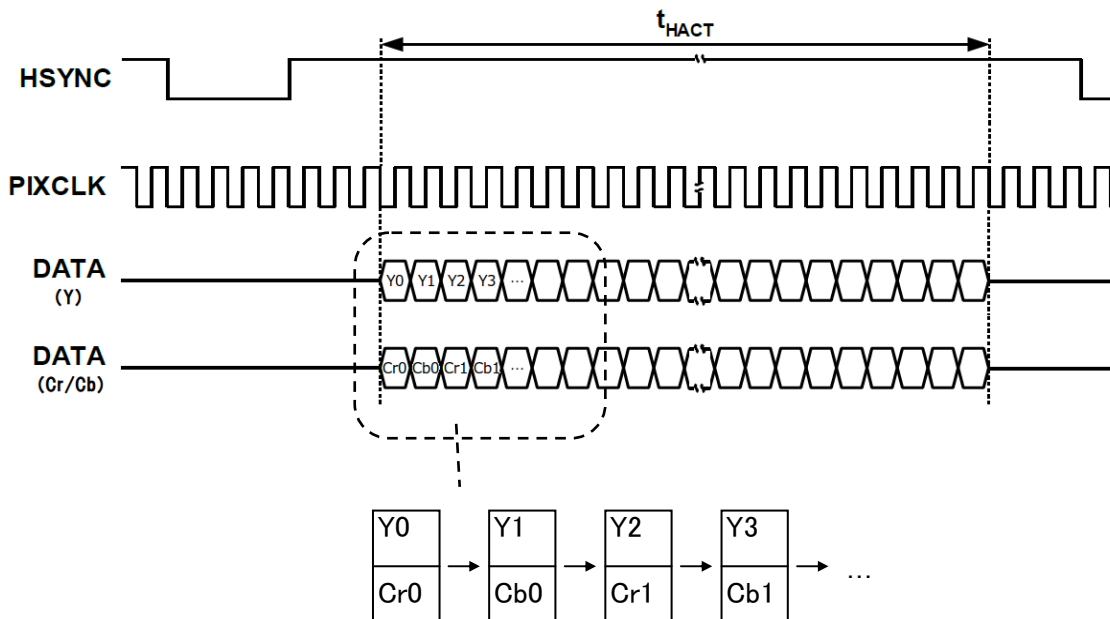


Fig. 3-3. Data Sequence in case of YCbCr4:2:2 parallel 16bit input

**Table 3. Parallel Data AC Characteristics Video Format Timing**

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC, frequency	$t_{VF}$	47	60	120	Hz
VSYNC, total lines	$t_{VTOT} = t_{VBLK} + t_{VACT}$	255 (*1)		1022	Lines
VSYNC, active lines	$t_{VACT}$	240	960	960	Lines
VSYNC, blanking	$t_{VBLK} = t_{VFP} + t_{VW} + t_{VBP}$	15 (*1)		300	Lines
VSYNC, front porch (*1)	$t_{VFP}$	6 (*1)		-	Lines
VSYNC, pulse width	$t_{VW}$	3		-	Lines
VSYNC, back porch	$t_{VBP}$	6 (*1)		-	Lines
HSYNC, total clocks	$t_{HTOT} = t_{HBLK} + t_{HACT}$	with Valid Input	346 (*2)	-	Clocks
		No Valid Input	364 (*2)	-	
HSYNC, active clocks	$t_{HACT}$	320	1280	1280	Clocks
HSYNC, blanking	$t_{HBLK} = t_{HFP} + t_{HW} + t_{HBP}$	with Valid Input	26 (*2)	-	Clocks
		No Valid Input	44 (*2)	-	
HSYNC, front porch	$t_{HFP}$	with Valid Input	10 (*2)	-	Clocks
		No Valid Input	10 (*2)	-	
HSYNC, pulse width	$t_{HW}$	with Valid Input	6	-	Clocks
		No Valid Input	6	511	
HSYNC, back porch	$t_{HBP}$	with Valid Input	10 (*2)	-	Clocks
		No Valid Input	28 (*2)	511	
CLOCK, rate	$1/t_{CP}$	24		103	MHz

\*1: When the number of VSYNC, active lines is less than 960, the minimum porch period is to be the following value or the value in the above table, whichever is larger.

V Back Porch  $\geq$  Ceiling[ (VOFFSETTOP \* 10us) / (H total clocks \* (1/PIXCLK freq)) ]

V Front Porch  $\geq$  Ceiling[ (VOFFSETBOT \* 10us) / (H total clocks \* (1/PIXCLK freq)) ]

\*2: When the number of HSYNC, active clocks is less than 1,280, the minimum porch period is to be the following value or the value in the above table, whichever is larger.

H Back Porch  $\geq$  Ceiling[ (300ns + (HOFFSETLEFT\*10ns)) / (1/PIXCLK freq) ]

H Front Porch  $\geq$  Ceiling[ (300ns + (HOFFSETRIGHT\*10ns)) / (1/PIXCLK freq) ]

VOFFSETTOP = voffset\_top\_pix

VOFFSETBOT = voffset\_bot\_pix

HOFFSETLEFT = hoffset\_left\_pix

HOFFSETRIGHT = hoffset\_right\_pix

Please refer to [Figure 4.1-3 Cropping and Offset].

In case of YCrCb 4:2:2 parallel 16bit data input, the values are to be twice the above calculated values.

**Supplementary Caution :**

Even within the range(Min to Max) in the table 3, a certain combination of video format timing may limit a certain value of the video format timing above.

It is advisable to consult us on the desired concrete values of video format timing.

### 4.1-3 Video Offset and Cropping

By setting horizontal, vertical video offset register (D1h-D5h), it enables to place the picture in the specific position on the display. The `hoffset_left_pix` and `hoffset_right_pix` registers are respectively set the display position from the right and left edge on a pixel unit basis.

The `voffset_top_pix` and `voffset_bot_pix` registers are respectively set the display position from the upper and bottom edge on a two-line unit basis. All the pixels other than display area are black.

The delay(in clocks) from HSYNC(VSYNC) assertion or Horizontal(Vertical) Valid aseertion (when using valid input) can be set by `hvid_delay`(0Dh-0Eh) registers and `vvid_delay`(0Ch) register(Cropping).

The horizontal sample delay `HVldDelay` (0Dh-0Eh) is always given in number of clocks, and the vertical sample delay `VVldDelay` (0Ch) is given in lines.

By offset register setting, the post-cropped picture can be adjust to place in the center of display area.

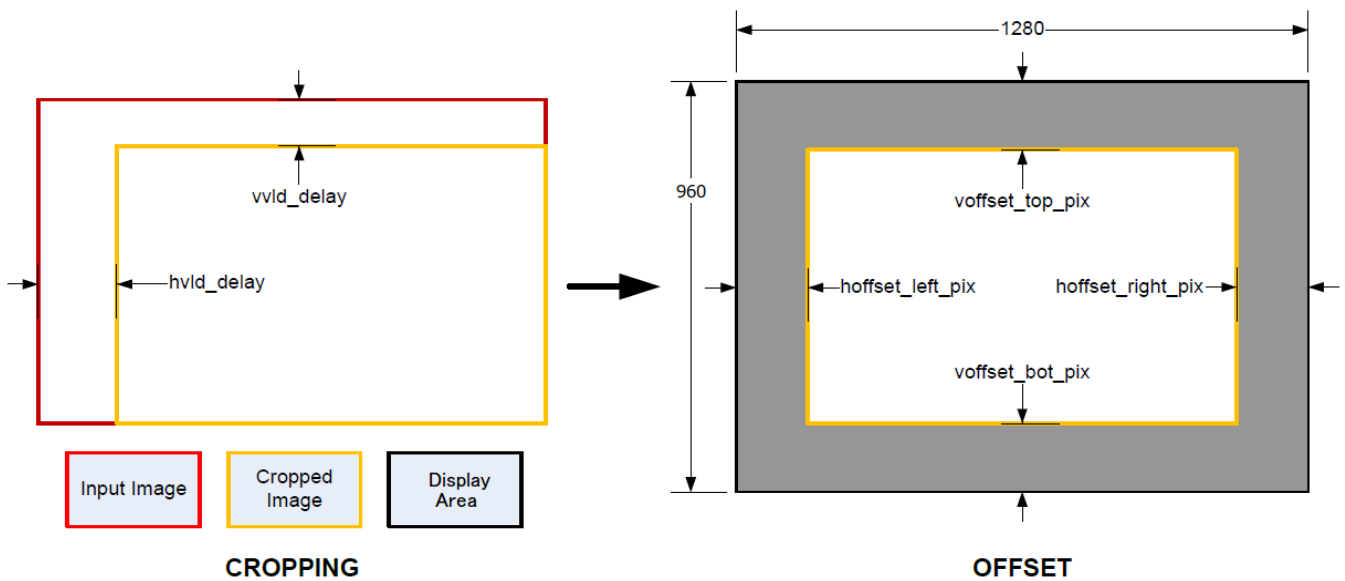


Fig. 4. Cropping and Offset

#### Supplementary Caution :

Other setting conditions may disable the vertical and horizontal offset functions.

When you use the offset register, it is advisable to consult us on the desired concrete values of video format timing.



#### 4.1-4 Scaling

The scaling engine is based on a fractional accumulator to support arbitrary input resolutions from 320 horizontal pixels to 1280 horizontal pixels and from 240 vertical pixels to 960 vertical pixels. The horizontal and vertical scaling coefficients (HScaleStep and VScaleStep) determine the scaling ratio. HScaleStep and VScaleStep register settings are determined as follows in round-up decimal values. (requires conversion to hexadecimal format)

$$XScaleStep = Ceiling \left[ 512 * \left[ \frac{Displayed Resolution}{Post Crop Input Resolution} \right] \right]$$

**Table 4. Scaling Setting Sample**

Input Resolution	Output Resolution	HScaleStep [dec]	VScaleStep [dec]
1280x960	VGA (640x480)	256	256
1280x960	qHD (960x540)	384	288
SVGA (800x600)	1280x960	820	820
720p (1280x720)	1280x960	512	683

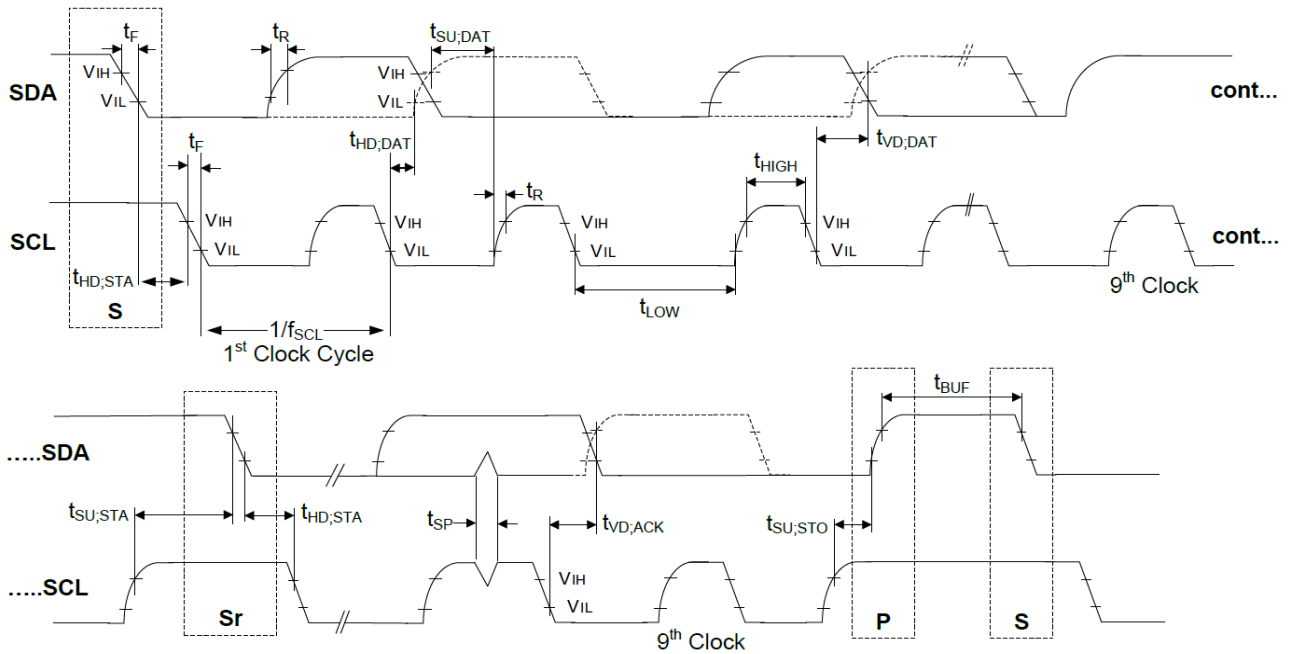
**Supplementary Caution :**

Other setting conditions may disable the scaling function.  
When you use the scaling function, it is advisable to consult us.

## 4.2 Control Interface

### 4.2-1 AC Characteristics of Interface Signal

This product is controlled by writing data in the control registers with I2C interface.  
The AC characteristics of interface signal are as follows.



\* For the definition of  $V_{IH}$  and  $V_{IL}$ , please refer to [4.5 Ratings].

**Fig. 5. I2C Interface Signal**

**Table 5. AC Characteristics (I2C Interface)**

Symbol	Parameter	Conditions	Standard-Mode		Fast-Mode		Unit
			Min.	Max.	Min.	Max.	
fSCL	SCL clock frequency		0	100	0	400	KHz
tHD;STA	hold time (& repeated) START condition	After this period, the first clock pulse is generated.	4	-	0.6	-	us
tLOW	LOW period of the SCL clock		4.7	-	1.3	-	us
tHIGH	HIGH period of the SCL clock		4	-	0.6	-	us
tSU;STA	set-up time for a repeated START condition		4.7	-	0.6	-	us
tHD;DAT	data hold time		5	-	5	-	ns
tSU;DAT	data set-up time		250	-	100	-	ns
tr	rise time of both SDA and SCL signals		-	1000	20+0.1Cb	300	ns
tf	fall time of both SDA and SCL signals		-	300	20+0.1Cb	300	ns
tSU;STO	set-up time for STOP condition		4	-	0.6	-	us
tBUF	bus free time between STOP and START condition		4.7	-	1.3	-	us
Cb	capacitive load for each bus line (depends on load and frequency)		-	400	-	400	pF
tVD;DAT	data valid time		-	3.45	-	0.9	us
tVD;ACK	data valid acknowledge time		-	3.45	-	0.9	us
tSP	pulse width of spikes that must be suppressed by the input filter		n/a	n/a	0	50	ns

**4.2-2 Protocol**

This FLC device is always considered a slave in the system and requires a clock to be provided to it for all I2C interface transactions.

**Start Condition :** A start condition is generated through the use of pulling down the SDA line while SCL is still high.

**Slave Address :** 7bit -- 0111110 (binary)

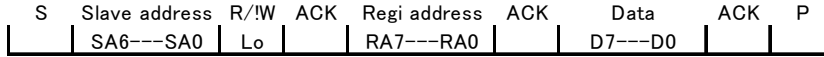
**R!/W bit :** The 8th bit -- If a READ is requested then the bit should be kept high, and if a WRITE is requested, the line is pulled down to a low-level signal.

**ACK bit :** The 9th bit -- the acknowledgment bit from the addressed device.  
If the addressed device receives its address and is not busy at that time it will respond by pulling the SDA line low and therefore signaling an acknowledgment. If an acknowledgment is detected by the issuing device, then the rest of the message can be sent.

**Stop Condition :** If SCL is kept high and SDA changes from low to high, the interface stops.

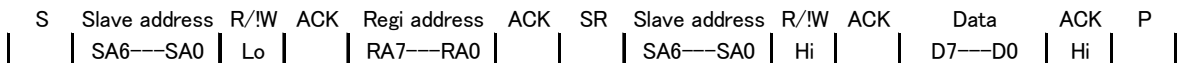
## Single Write Protocol

A START signal must be presented first. This is when the SDA line is pulled low while the SCL line is kept high. The first byte sent is always the slave address for the qHD panel's I2C interface (0111 110b) followed by the R/W bit(Lo). An acknowledge (ACK) is returned from the receiving device after each byte sent by pulling the SDA line low for one clock. The clock is still provided by the master device, which is never the qHD panel display. The second byte sent in the write transactions is the qHD panel's 8-bit register address that will be written. After the register address is sent, the byte to be written is sent. The master keeps control of the bus and delivers the byte to be written.



## Single Read Protocol

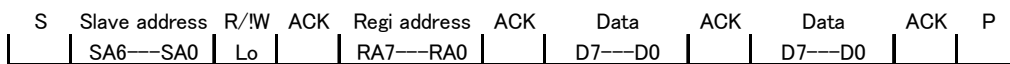
After a START, the slave address and R/W(Lo) are sent. After an ACK is returned from the receiving device, the register address to be read is sent. Again after an ACK is returned from the receiving device, a START signal is presented again and the slave address is sent followed by the R/W bit(Hi). After an ACK is returned, the device reads the byte data but not return an ACK. Then, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.



\* SR : Restart

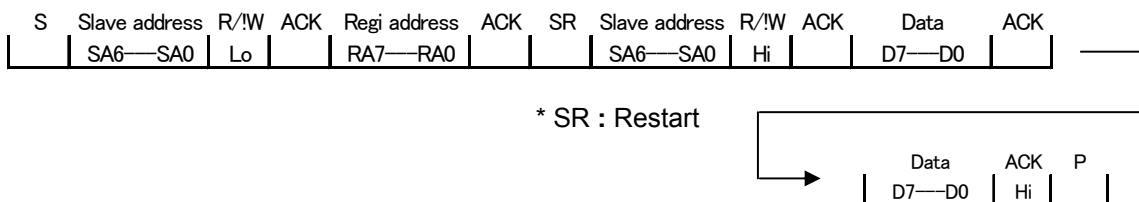
## Multi-Write Protocol

Similar to single write protocol, after transactions of a START, the slave address, R/W(Lo), an ACK, and byte data in that order, by continuously outputting data, the register address is auto-incremented for each byte write. After all data are written in the necessary addresses, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.



## Multi-Read Protocol

Similar to single read protocol, after transactions of a START, the slave address, R/W(Lo), an ACK, the register address, a START(SR), the slave address, R/W(Hi) and an ACK in that order, by continuously reading data, the register address in the device is auto-incremented and the data is output. After all data are read in the necessary addresses, not returning an ACK, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.

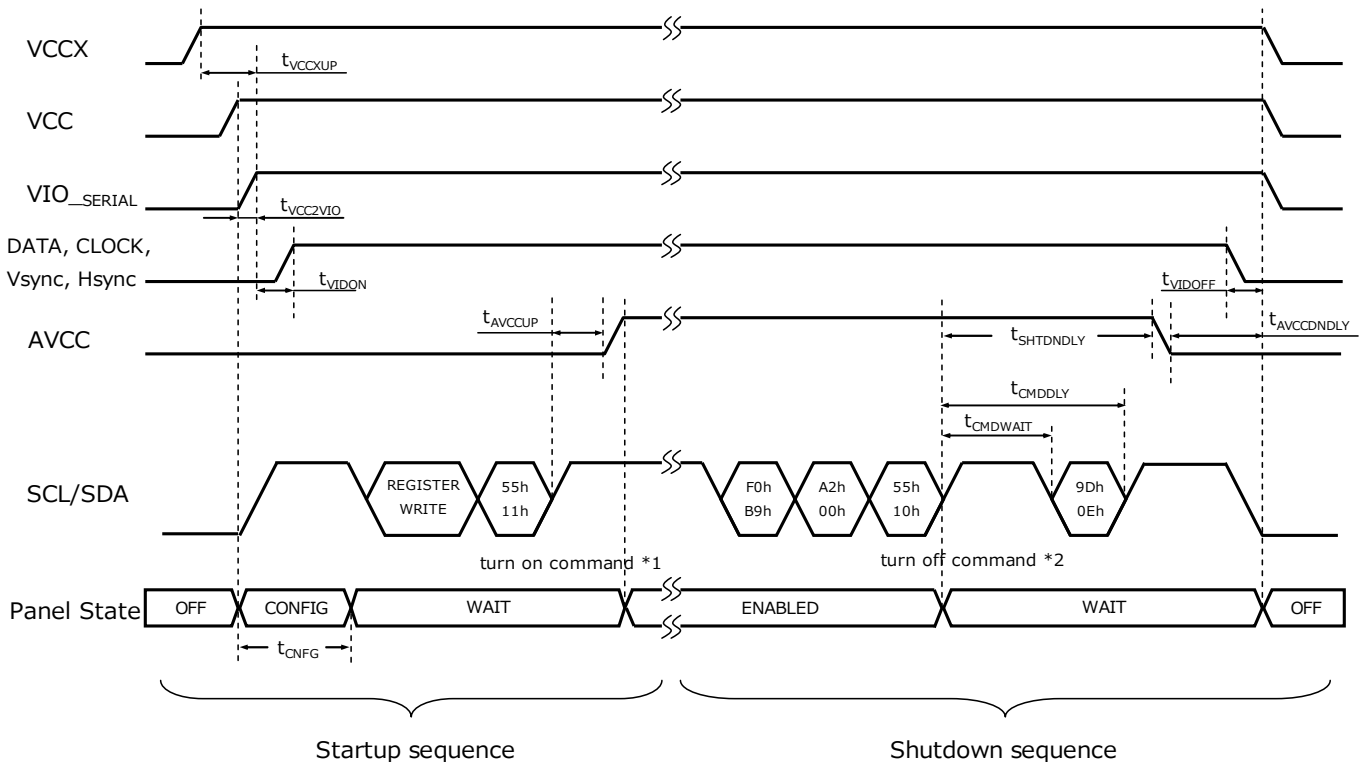


### 4.3 Control Sequence Requirements

The following timing/sequence requirements must be met during Start-up, Shut-down, Sleep and Wake-up to avoid damages to the display panel.

#### 4.3-1 Start-up Sequence Requirements

The VCCX power supply must be present before the VCC power supply is present. After the VCCX power supply is present, the VCC, VIO\_serial must be present for a time period of  $t_{VCCXUP}$ . No precedence on which supply, the VCC or VIO\_serial, is present earlier, however, the both of power supplies must be present for a time period of  $t_{VCC2VIO}$ . After the VCC voltage supply is present and in specification, the display panel will load default register values from non-volatile memory to RAM for a time period of  $t_{CNFG}$ . During this time period, the two-wire serial interface is ignored. Although the voltage supplies (VCC, VCCX, VIO\_serial) can be present simultaneously, the  $t_{CNFG}$  starts when the VCC power supply is in specification. After the  $t_{CNFG}$  period, the two-wire serial interface will be active, which enables register setting for all commands other than a turn-on command, if necessary. After a time period of  $t_{VIDON}$  since the voltage supplies (VCC, VCCX, VIO\_serial) is present, all the video signals (DATA, CLOCK, Vsync, Hsync) must be present. After the VCC, VCCX, VIO\_serial supplies are present followed by stable presence of all the video signals (DATA, CLOCK, Vsync and Hsync), the turn-on command must be present. The turn-on command contains the requirement that the AVCC supply must be present after a time period of  $t_{AVCCUP}$ . After the turn-on command is complete, the display panel starts image display.



\*1 turn on command  
 Register Index : Data Value  
 (# 1) 55h : 11h  
 (# 2)  $t_{AVCCUP}$   
 (# 3) AVCC Supply

\*2 turn off command  
 Register Index : Data Value  
 (# 1) F0h : B9h  
 (# 2) A2h : 00h  
 (# 3) 55h : 10h  
 (# 4)  $t_{CMDWAIT}$   
 (# 5) 9Dh : 0Eh

Fig. 6-1. Start-up/Shut-down Sequence

### 4.3-2 Shut-down Sequence

In case of shut-down of the display, the turn-off command must be present through the serial interface, before the voltage supplies are stopped.

After the turn-off command is present, each power supply including the AVCC and the video signals(DATA, CLOCK, Vsync, Hsync) must be continuously supplied for a time period of  $t_{SHTDNDLY}$ . Afterwards, the AVCC power supply is stopped first, and then the video signals(DATA, CLOCK, Vsync, Hsync) must be stopped.

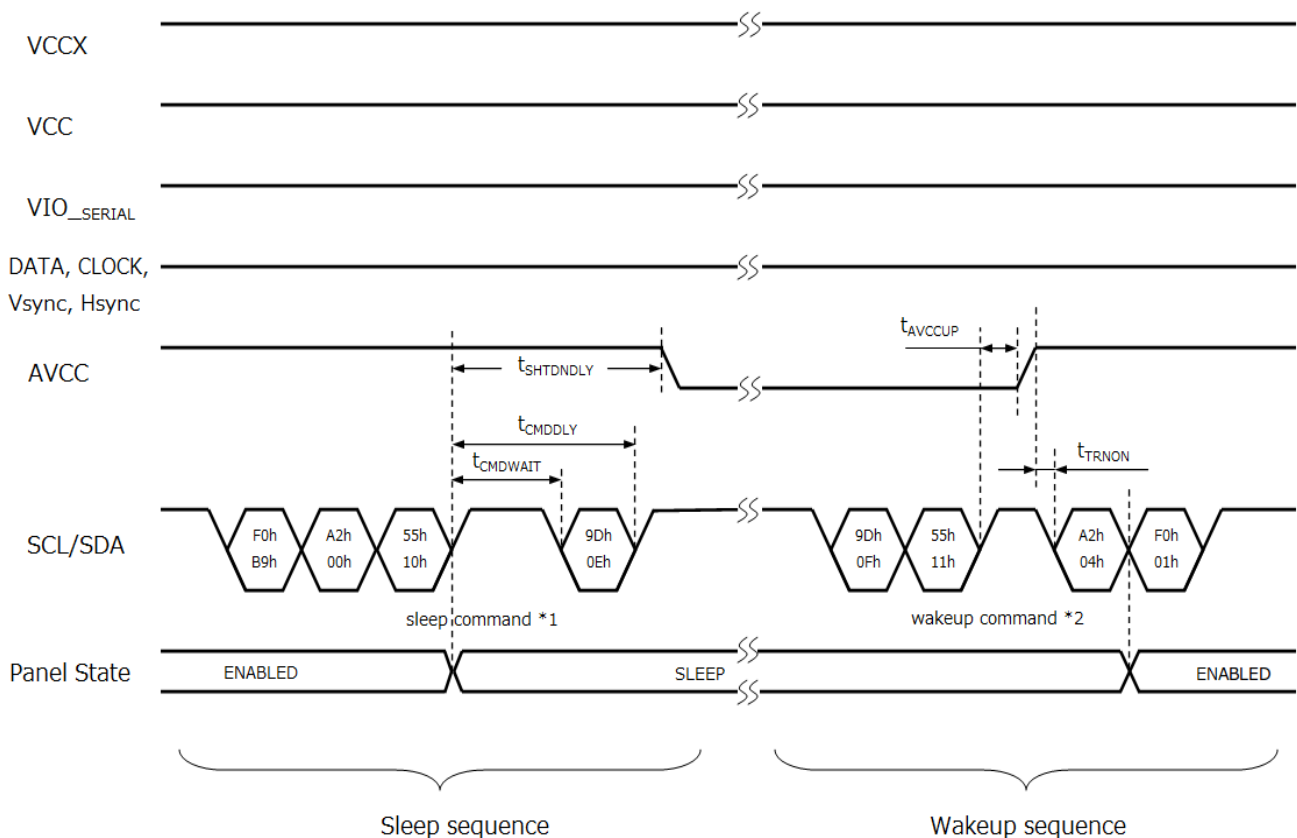
After a time period of  $t_{AVCCDNDLY}$ , the voltage supplies (VCC, VCCX, VIO\_serial) must be stopped. Please note that the video signals(DATA, CLOCK, Vsync, Hsync) must be stopped a time period of  $t_{VIDOFF}$  or earlier before the voltage supplies (VCC, VCCX, VIO\_serial) is stopped.

### 4.3-3 Sleep Sequence

To set the display to the sleep state, the sleep command below must be present through the serial interface. Afterwards, the AVCC power supply must be stopped after the  $t_{SHTDNDLY}$  time period.

### 4.3-4 Wake-up Sequence

To enable the display from the sleep state, the wake-up command below must be present through the serial interface. The wake-up command contains the requirement that the AVCC supply must be present after a time period of  $t_{AVCCUP}$ .



\*1 sleep command  
 Register Index : Data Value  
 (# 1) F0h : B9h  
 (# 2) A2h : 00h  
 (# 2) 55h : 10h  
 (# 4) tCMDWAIT  
 (# 5) 9Dh : 0Eh

\*2 wake-up command  
 Register Index : Data Value  
 (# 1) 9Dh : 0Fh  
 (# 2) 55h : 11h  
 (# 3) tAVCCUP  
 (# 4) AVCC supply  
 (# 5) tTRNON  
 (# 6) A2h : 04h  
 (# 7) F0h : 01h

Fig. 6-2. Sleep/Wake-up Sequence

**Table 6. AC Characteristics ( Control Sequence Timing)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
<b>Start-up Sequence / Wake-up Sequence</b>					
Time from VCCX supply to VCC,VIO_serial supply	$t_{VCCXUP}$	0	-	5	ms
Time from VCC supply to VIO_serial supply	$t_{VCC2VIO}$	-1	-	1	ms
Time from VCC supply to when Configuration is finished.	$t_{CNFG}$		-	100	ms
Time from VCCX,VCC,VIO_serial supply to when video signals are supplied.	$t_{VIDON}$	0	-	-	us
Time after the turn-on command(#1) to when DAVCC is supplied(*1).	$t_{AVCCUP}$	6	-	-	video field
Time from DAVCC supply(*2) to when the turn-on command(#5) is started.	$t_{TRNON}$	0	-	-	us
<b>Shut-down Sequence / Sleep Sequence</b>					
Time of the designated waiting period in the turn-off command.	$t_{CMDWAIT}$	1.5	-	-	ms
Time after the shut-down command(#2) to when the turn-off	$t_{CMDDLY}$	-	-	3	ms
Time after the turn-off command(#2) to when DAVCC is stopped(*2).	$t_{SHTDNDLY}$	$t_{CMDDLY}$	-	-	ms
Time from stop of video signals to stop of VCCX,VCC,VIO_serial supplies.	$t_{VIDOFF}$	0	-	-	us
Time from stop of DAVCC(*1) to stop of VCCX,VCC,VIO_serial supplies.	$t_{AVCCDNDLY}$	$200 + t_{VIDOFF}$	-	-	us

Note 1. The definitions of \*1 & \*2 in the table above with regard to DAVCC are as follows.

(\*1) Point where the AVCC achieves 0.5V.

(\*2) Point where the AVCC achieves the minimum rating in volt.

Note 2. All the definitions in the table above with regard to VCC, VCCX, VIO\_serial mean the point where the voltage achieves the minimum rating.

#### Supplementary Precaution Statements

- \* To prevent the display image from being distorted or other failure, the stable video signals must be present during the time from when turn-on command is present to when turn-off command is complete.
- \* if the turn-on command is present during a period other than the time from the Vsync to {the value set in the vld\_delay register(0Ch) - 2} line(TBD), the vertical position of the image primarily displayed may be shifted from the proper position.
- \* When each register is written with a certain value, the value reflects the operation of the display.

#### 4.4 Pin Assignments

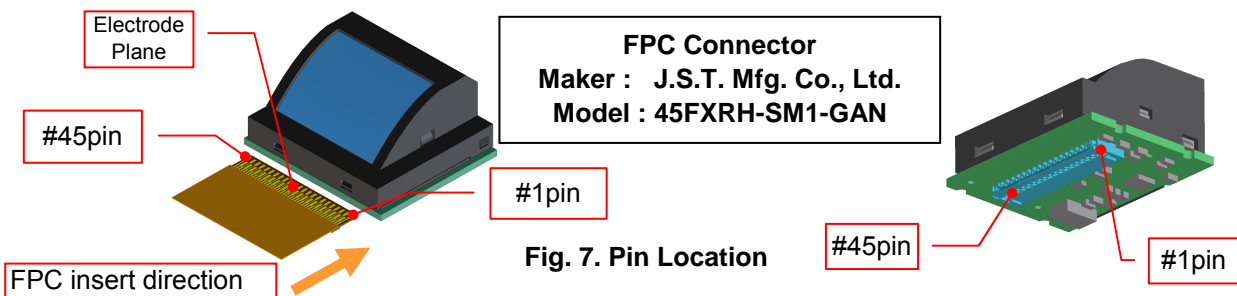
Table 7. Pin Assignments

No	Name	I/O	Power Supply	Function		
				24bit RGB	24bit YCbCr(4:4:4)	16bit YCbCr(4:2:2)
1,2	GND	NA	NA	Ground		
3,4,5	VCC(*2)	NA	NA	Panel Core Power Supply (+1.8V)		
6	GND	NA	NA	Ground		
7	VCCX	NA	NA	Panel / EEPROM Power Supply (+3.3V)		
8	N.C.	NA	NA	* Open or directly connect to VCC		
9	VIO_Serial	NA	NA	Serial Interface I/O Power Supply (1.8V to 3.3V)		
10	CLOCK	I	1.8V	Video Data Clock		
11	VSYNC	I	1.8V	Vertical Synch Signal		
12	HSYNC	I	1.8V	Horizontal Synch Signal		
13	VALID	I	1.8V	Valid Signal (* If non-use : GND)		
14	GND	NA	NA	Ground		
15	DATA 23	I	1.8V	Blue[7]	Cr[7]	GND
16	DATA 22	I	1.8V	Blue[6]	Cr[6]	GND
17	DATA 21	I	1.8V	Blue[5]	Cr[5]	GND
18	DATA 20	I	1.8V	Blue[4]	Cr[4]	GND
19	DATA 19	I	1.8V	Blue[3]	Cr[3]	GND
20	DATA 18	I	1.8V	Blue[2]	Cr[2]	GND
21	DATA 17	I	1.8V	Blue[1]	Cr[1]	GND
22	DATA 16	I	1.8V	Blue[0]	Cr[0]	GND
23	DATA 15	I	1.8V	Green[7]	Cb[7]	Cb[7] / Cr[7]
24	DATA 14	I	1.8V	Green[6]	Cb[6]	Cb[6] / Cr[6]
25	DATA 13	I	1.8V	Green[5]	Cb[5]	Cb[5] / Cr[5]
26	DATA 12	I	1.8V	Green[4]	Cb[4]	Cb[4] / Cr[4]
27	DATA 11	I	1.8V	Green[3]	Cb[3]	Cb[3] / Cr[3]
28	DATA 10	I	1.8V	Green[2]	Cb[2]	Cb[2] / Cr[2]
29	DATA 9	I	1.8V	Green[1]	Cb[1]	Cb[1] / Cr[1]
30	DATA 8	I	1.8V	Green[0]	Cb[0]	Cb[0] / Cr[0]
31	DATA 7	I	1.8V	Red[7]	Y[7]	Y[7]
32	DATA 6	I	1.8V	Red[6]	Y[6]	Y[6]
33	DATA 5	I	1.8V	Red[5]	Y[5]	Y[5]
34	DATA 4	I	1.8V	Red[4]	Y[4]	Y[4]
35	DATA 3	I	1.8V	Red[3]	Y[3]	Y[3]
36	DATA 2	I	1.8V	Red[2]	Y[2]	Y[2]
37	DATA 1	I	1.8V	Red[1]	Y[1]	Y[1]
38	DATA 0	I	1.8V	Red[0]	Y[0]	Y[0]
39	GND	NA	NA	Ground		
40,41	AVCC	NA	NA	Panel Analog / LED Power Supply (+5V)		
42	GND	NA	NA	Ground		
43	SDA	IO	VIO_Serial	Serial Interface Data I/O		
44	SCL	I	VIO_Serial	Serial Interface Clock Input		
45	GND	NA	NA	Ground		

\*1: A mapping of video data signal for DATA0~23 can be changed.

The details are referred to in [5.Configuration Register Settings] .

\*2: It is recommendable to put a 10uF or larger decoupling capacitor to the VCC on a operation circuit side.





## 4.5 Ratings

**Table 8-1. Absolute Maximum Ratings**

Parameter	Absolute Maximum Rating		Unit
	Min.	Max.	
VCCX	-0.5	3.5	V
VCC	-0.5	1.9	V
AVCC	-0.5	5.3	V
VIO <sub>serial</sub>	-0.5	3.5	V
Voltage on any Video Input Pin	-0.4	VCCX + 0.4	V
Voltage on any Serial Input Pin	-0.4	VIO <sub>serial</sub> +0.4	V

**Table 8-2. DC Characteristics**

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	VCCX	*1	3.1	3.3	3.5	V
	VCC	*1	1.7	1.8	1.9	
	AVCC		4.7	5.0	5.3	
	VIO <sub>serial</sub>		1.7	3.3	3.5	
*1: While operating, the VCCX and VCC must fulfill the following conditions. $VCCX \leq (VCC \times 2) [V]$						
Input Voltage	VIH	For all video inputs	0.74*VCC			V
		For all serial inputs	0.74*VIO <sub>serial</sub>			
	VIL	For all video inputs			0.25*VCC	
		For all serial inputs			0.25*VIO <sub>serial</sub>	
Input Capacitance	IC	For all inputs 3.3Vp-p, f=5MHz		6	12	pF
Input Leakage Current	IIL	VI = VIL	-10			uA
	IIH	VI = VIH			10	
Average panel operating supply current <Measurement Conditions> VCC=1.80V, VCCX=3.30V, AVCC=5.00V, VIO <sub>serial</sub> =3.30V, Input Resolution=1280x720 (16bit parallel), Display Resolution=1280*720 (No Scaling), Image = White Raster CLOCK =75MHz, Field Frequency=60Hz At room temp. and under normal conditions.	I <sub>VCCX</sub>	VCCX=3.30V VCC=1.80V AVCC=5.00V VIO <sub>serial</sub> =3.30V		7	TBD	mA
	I <sub>VCC</sub>	Input Video Data= 1280x960(24bit RGB) Display Resolution= 1280*960		180	TBD	
	I <sub>AVCC</sub>	Image = White Raster CLOCK =75MHz, Field Frequency=60Hz Gamma = 2.1		2	TBD	
	I <sub>VIO<sub>serial</sub></sub>	At room temp. and under normal conditions.		0.1	TBD	

### 4.6 Electronic Circuit Diagram

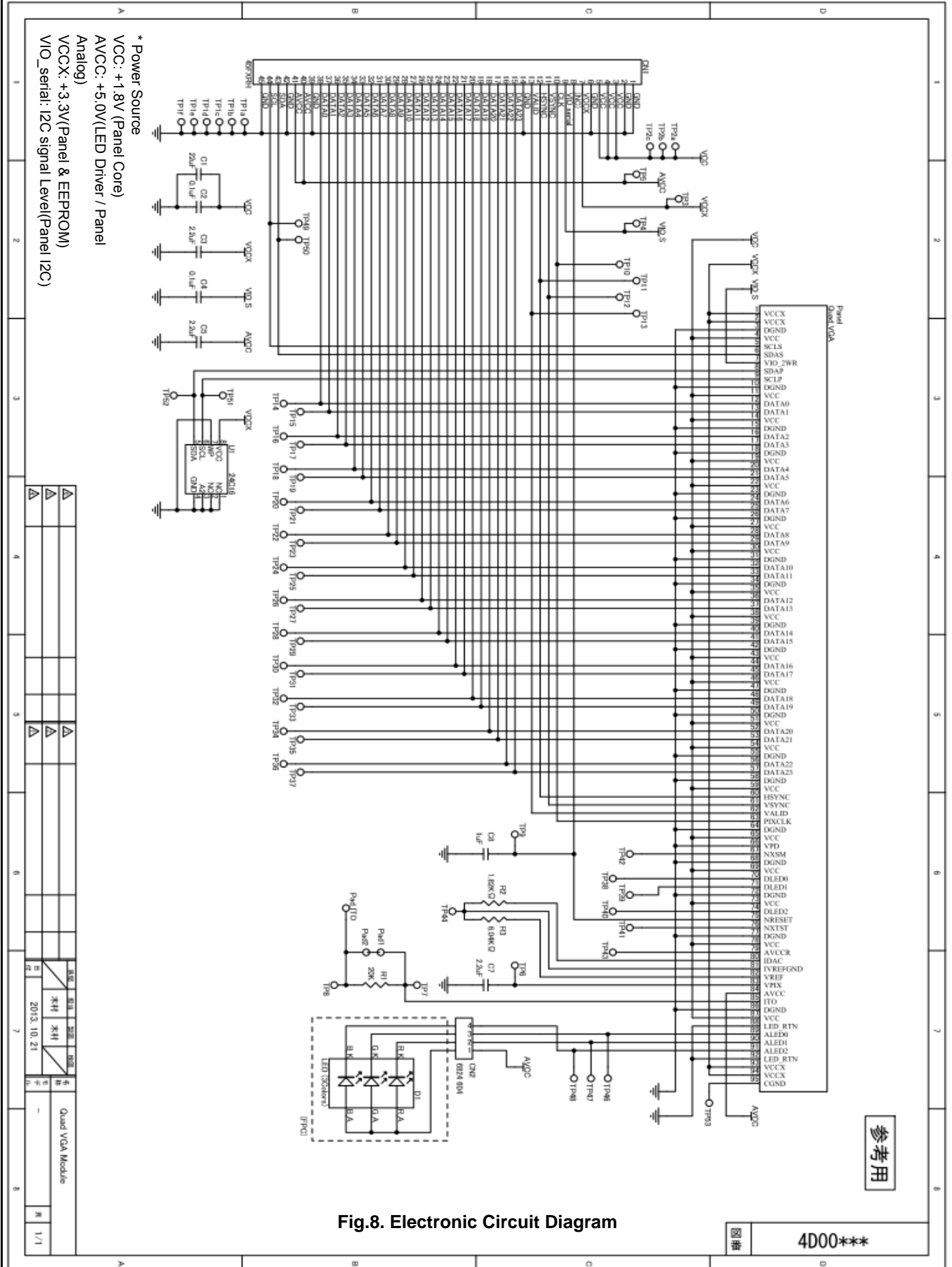


Fig.8. Electronic Circuit Diagram

参考用

4D00\*\*\*

图例

## 5. Configuration Register Settings

### Register Index : 00h

Bit	7	6	5	4	3	2	1	0
Meaning	dither_mode[3:0]				Res			
Value(e.g.)	0001				0001			

dither\_mode: Select dither mode

4'h1=1/2bit Spatial Dither , 1/4bit Temporal Dither

4'h2=1/2bit Temporal Dither, 1/4bit Spatial Dither

4'h3=1/2bit Spatial Dither

4'h5=Reserved (Not Available)

4'h6=Reserved (Not Available)

other= No dither / Input data rounded to 7-bit values

Res: Reserved

The above "Res" register value must be set to 0001b.

\* The following "Res" register values must be set to the value instructed as e.g. value.

### Register Index : 01h

Bit	7	6	5	4	3	2	1	0
Meaning	cspace_sel	channel_map[2:0]			data_channel[1:0]		data_seq[1:0]	
Value(e.g.)	0	000			00		00	

cspace\_sel: Color Space Select

0 = RGB

1 = YCrCb

channel\_map: select mapping of data channel to color information, dependent on the data channel setting according to the following table.

channel_map	24-bit RGB			24-bit YCbCr			16-bit YCbCr		
	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]
0h	Blue	Green	Blue	Cr	Cb	Y	-	Cb/Cr	Y
1h	Green	Red	Green	Cb	Y	Cr	-	Y	Cb/Cr
2h	Red	Blue	Red	Y	Cr	Cb	Cb/Cr	Y	-
3h	Red	Green	Red	Y	Cb	Cr	Y	Cb/Cr	-
4h	Green	Blue	Green	Cb	Cr	Y	Cb/Cr	-	Y
5h	Blue	Red	Blue	Cr	Y	Cb	Y	-	Cb/Cr

data\_channel: select data interface

00=RGB/ YCbCr -24bit data interface

01=YCbCr -16bit data interface

other=Reserved (Setting is Not Available)

data\_seq: data sequence of color information

DataSequence	24-bit RGB	24-bit YCbCr	16-bit YCbCr
00	[R][G][B]	[Y][Cr][Cb]	Reserved (Setting : N/A)
01	Reserved (Setting : N/A)	Reserved (Setting : N/A)	[Y0Cr0] [Y1Cb0]
10	Reserved (Setting : N/A)	Reserved (Setting : N/A)	Reserved (Setting : N/A)
11	Reserved (Setting : N/A)	Reserved (Setting : N/A)	Reserved (Setting : N/A)

**Register Index : 02h**

Bit	7	6	5	4	3	2	1	0
Meaning	vsync_pol	hsync_pol	valid_pol	Res			sync_mode	
Value(e.g.)	1	1	0	000			00	

vsync\_pol: Vertical sync polarity  
0=Active High, 1=Active Low

hsync\_pol: Horizontal sync polarity  
0=Active High, 1=Active Low

valid\_pol: Valid sync polarity  
0=Active High, 1=Active Low

sync\_mode : Selects data sampling mode.  
00=Use VALID inputs for valid video timing.  
01=Use HSYNC and VSYNC inputs, valid timing specified from valid\_delay registers.  
10 and 11=Reserved (n/a)

**Register Index : 06h**

Bit	7	6	5	4	3	2	1	0
Meaning	Res					vscale_step[10:8]		
Value(e.g.)	0000 0					010		

**Register Index : 07h**

Bit	7	6	5	4	3	2	1	0
Meaning	vscale_step[7:0]							
Value(e.g.)	0000 0000							

vscale\_step: Vertical scaling coefficient [range: 0-1024d]

**Register Index : 09h**

Bit	7	6	5	4	3	2	1	0
Meaning	Res					hscale_step[10:8]		
Value(e.g.)	0000 0					010		

**Register Index : 0Ah**

Bit	7	6	5	4	3	2	1	0
Meaning	hscale_step[7:0]							
Value(e.g.)	0000 0000							

hscale\_step: Horizontal scaling coefficient [range: 0-1024d]

**Register Index : 0Ch**

Bit	7	6	5	4	3	2	1	0
Meaning	vvld_delay[7:0]							
Value(e.g.)	0000 0000							

vvld\_delay: Vertical Valid Delay specified in number of lines.

sync\_mode=00 : Delay from vertical valid assertion to video data sampling.  
The setting value will crop the video.

sync\_mode=01 : Delay from VSync assertion to video data sampling.  
The value should nominally be set to tVW+tVBP.  
The part of value(lines) beyond the tVW+tVBP will crop the video.  
(Refer to Fig.3-1 & Fig.4)

**Register Index : 0Dh**

Bit	7	6	5	4	3	2	1	0
Meaning	Res						hvld_delay[9:8]	
Value(e.g.)	0000 00							

hvld\_delay: Upper bits of horizontal valid delay \* Refer to register index 0Eh below.

**Register Index : 0Eh**

Bit	7	6	5	4	3	2	1	0
Meaning	hvld_delay[7:0]							
Value(e.g.)								

hvld\_delay : Horizontal Valid Delay specified in number of clocks.

sync\_mode=00 : Delay from horizontal valid assertion to video data sampling  
The setting value will crop the video.

sync\_mode=01 : Delay from HSync assertion to video data sampling -2.  
The value should nominally be set to tHW+tHBP-2.  
The part of value(clocks) beyond the tHW+tHB-2 will crop the video.  
(Refer to Fig.3-2 & Fig.4)

**Register Index : 0Fh-17h**

Index	Value(e.g.)	7	6	5	4	3	2	1	0
0Fh	00h	color_space_bus (cs <sub>11</sub> )							
10h	00h	color_space_bus (cs <sub>12</sub> )							
11h	00h	color_space_bus (cs <sub>13</sub> )							
12h	00h	color_space_bus (cs <sub>21</sub> )							
13h	00h	color_space_bus (cs <sub>22</sub> )							
14h	00h	color_space_bus (cs <sub>23</sub> )							
15h	00h	color_space_bus (cs <sub>31</sub> )							
16h	00h	color_space_bus (cs <sub>32</sub> )							
17h	00h	color_space_bus (cs <sub>33</sub> )							

color\_space\_bus: Parameters to change color space setting.

\* See the Color Space Conversion Equation in Figure 9.

**Register Index : 18h-1Ah**

Index	Value(e.g.)	7	6	5	4	3	2	1	0
18h	00h	color_offset_bus (O <sub>1</sub> )							
19h	00h	color_offset_bus (O <sub>2</sub> )							
1Ah	00h	color_offset_bus (O <sub>3</sub> )							

color\_offset\_bus: Parameters to change color space setting.

The YCbCr values are basically converted to RGB values displayed by the values highlighted in yellow in the following equation. By setting the values highlighted in blue, the color space conversion can be available.

$$\begin{bmatrix} R_o \\ G_o \\ B_o \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128 + cs_{11} & 0 + cs_{12} & 175 + cs_{13} \\ 128 + cs_{21} & -42 + cs_{22} & -90 + cs_{23} \\ 128 + cs_{31} & 222 + cs_{32} & 0 + cs_{33} \end{bmatrix} \cdot \begin{bmatrix} Y_I + O_1 \\ Cb_I - 128 + O_2 \\ Cr_I - 128 + O_3 \end{bmatrix}$$

**Fig. 9. Color Space Conversion Equation**

**Register Index : 50h**

Bit	7	6	5	4	3	2	1	0
Meaning	Res		led_bright_ratio[5:0]					
Value(e.g.)	11		3Fh					

led\_bright\_ratio: LED brightness for display lighting

Brightness is divided into 64 scales and can be set.

0h= minimum brightness (1/64)

∧

3Fh=maximum brightness (64/64)

**Register Index : D0h**

Bit	7	6	5	4	3	2	1	0
Meaning	Res						vflip	hflip
Value(e.g.)	0000 00						1	1

vflip: Display vertical flip

0= disable display vertical flip mode

1= enable display vertical flip mode

hflip: Display horizontal flip

0= disable display horizontal flip mode

1= enable display horizontal flip mode



**Fig. 10. Display position at vflip=1, hflip=1**

**Register Index : D1-D5h**

Index	Value(e.g.)	7	6	5	4	3	2	1	0	
D1h		voffset_top_pix[7:0]								
D2h		voffset_bot_pix[7:0]								
D3h		hoffset_left_pix[7:0]								
D4h		hoffset_right_pix[7:0]								
D5h		hoffset_right_pix[9:8]		hoffset_left_pix[9:8]		voffset_bot_pix[9:8]		voffset_top_pix[9:8]		

voffset\_top\_pix: Vertical offset from the top edge

The offset line from the top edge of the vertical 960 lines to the top edge of picture display (Unit : 2line)

voffset\_bot\_pix: Vertical offset from the bottom edge

The offset line from the bottom edge of the vertical 960 lines to the bottom edge of picture display (Unit : 2line)

hoffset\_left\_pix: Horizontal offset from the left edge

The offset pixel from the left edge of the horizontal 1280 pixels to the left edge of picture display (Unit : pixel)

hoffset\_right\_pix: Horizontal offset from the right edge

The offset pixel from the right edge of the horizontal 1280 pixels to the right edge of picture display (Unit : pixel)

**Register Index : CEh**

Bit	7	6	5	4	3	2	1	0
Meaning	Res				gamma_val[3:0]			
Value(e.g.)	0000				9h			

gamma\_val: Gamma correction value select (1.7 ~ 2.2)

4'h5=gamma 1.7

4'h6=gamma 1.8

4'h7=gamma 1.9

4'h8=gamma 2.0

4'h9=gamma 2.1

4'hA=gamma 2.2

other=Reserved(Not Available)

Note) The gamma value affects the display's luminance and contrast ratio.

## 6.Display Panel Specification

### 6.1 Optical Characteristics

**Table 9. Optical Characteristics (at Room Temp.)**

Item	Conditions	Min.	Typ.	Max.	Unit	
Center Luminance	White Raster Image Measure the luminance of the center of the display.	200	210		cd/m <sup>2</sup>	
Contrast Ratio	White Raster / Black Raster Image Measure the luminance ratio of the center of the panel.	TBD	TBD		-	
xy Chromaticity	White Raster Image Measure the chromaticity of the center of the panel.	x	0.297	0.312	0.327	-
		y	0.314	0.329	0.344	-

Note : Measurement conditions of the optical characteristics are as follows.

#### [Measurement Conditions]

Supply Voltage : VCC=1.80V, VCCX=3.30V, VIO\_serial=3.30V,  
AVCC=5.00V

Video Signal Input : RGB 24bit / Resolution(1280 x 960)  
White R=FFh, G=FFh, B=FFh  
Black R=00h, G=00h, B=00h

Gamma Correction : 2.1

LED brightness register : Setting at maximum (3Fh)

Clock / Field Frequency : Clock= 75MHz / Field Frequency=60Hz

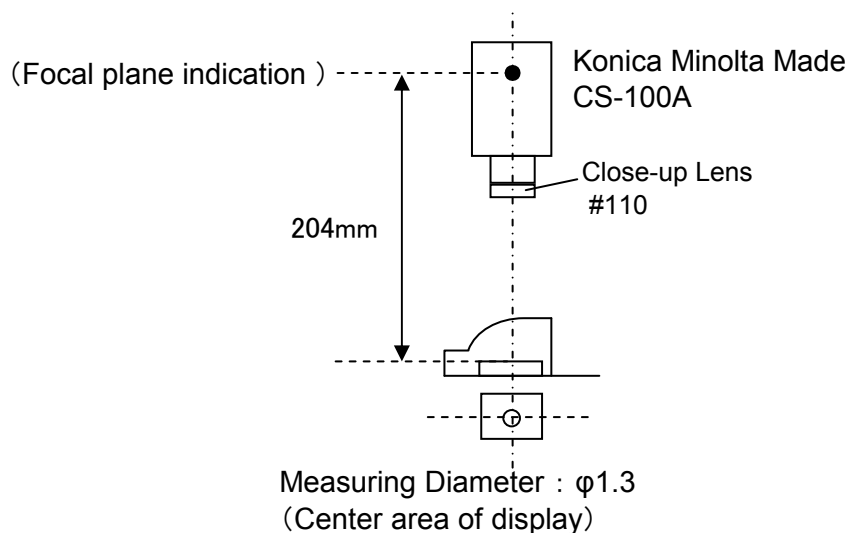
Temperature : Room Temp. (25°C Typ.)

Luminance & Color Meter: CS-100A manufactured by Konica minolta

xy Chromaticity : Measured on white image

Luminance : Measured on white image

Contrast Ratio : Calculated by white luminance above vs  
black luminance which is measured on white image



**Fig.11. Optical Measurement**



## 6.2 Visual Specifications

### 6.2-1 Display area visual defects

Conditions of inspection

At room temperature and normal humidity, inspect the display by microscope of 10 magnification focusing on the display focal plane.

Dither mode setting : 1/2bit spatial and 1/4bit temporal dither Gamma correction setting : 2.1

Color space/ Color offset register setting : 0h(All setting)

Input Signal Level 0%: (R,G,B)=(00h,00h,00h), 100%: (R,G,B)=(FFh,FFh,FFh)

**Table 10. Display area visual defects**

Subject Area	Defect Item	Defect Size (S) [Unit : pixel]	Allowable Quantity[Unit : pcs]
Display area	Bright/White Spot (Except for high bright spots)	$S \leq 1$ 1 pixel or smaller	Any quantity is allowable.
		$1 < S \leq 3$ Larger than 1 pixel & 3 pixels or smaller	3
		$3 < S \leq 6$ Larger than 3 pixels and 6 pixels or smaller	1
		$6 < S$ Larger than 6 pixels	Any quantity is NOT allowable.
Display area	Particle	$S \leq 1$ 1 pixel or smaller	Any quantity is allowable.
		$1 < S \leq 3$ Larger than 1 pixel & 3 pixels or smaller	3
		$3 < S \leq 6$ Larger than 3 pixels and 6 pixels or smaller	1
		$6 < S$ Larger than 6 pixels	Any quantity is NOT allowable.
Display area	Dark Spot	Any dark spot that degrades the quality of display is NOT allowable. Please refer to the following criteria only as a guide.	
		$S \leq 1$ 1 pixel or smaller	Any quantity is allowable.
		$1 < S \leq 3$ Larger than 1 pixel & 3 pixels or smaller	3
		$3 < S \leq 6$ Larger than 3 pixels and 6 pixels or smaller	1
		$6 < S$ Larger than 6 pixels	Any quantity is NOT allowable.
Display area	Bright Line		Any line is NOT allowable.

Note 1) Definition of display area is shown in Figure 12.

Note 2) The Dark Spot means pixels which show fixed black or gray color due to electrical dysfunction.

Note 3) Each defect must not be mutually adjacent to other by at least 2 pixels regardless of the number of defects.

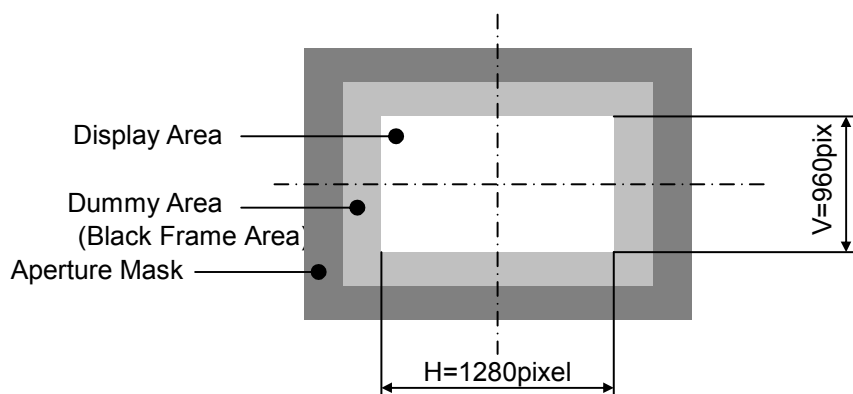


Fig. 12. Display area

## 6.2-2 Product appearance defects

**Table 11-1. Appearance defects**

Item		Specification
Plastic parts appearance	Scratch	Should not affect the product performance.
	Dirt	Should be removable easily.
	Stain	Should not affect the product performance.
	Deformation	Should not affect the product performance.
Other appearance		Should not affect the product performance.

**Table 11-2. Illuminator optical film defects**

Item	Specification
Outside surface	Removable particles are accepted. Unremovable defects (for instance, scratch) should be in spec of the inside surface.
Inside surface	Should not degrade display image (*1).

\*1: Any defects that cannot be detected with focusing on the display focal plane as described in Fig. 11 are ignorable.

The inspection conditions are the same as the conditions defined in [6.2-1 Display area visual defects].

## 7.Serial Number

### 1) Serial No

X X XXXXXX X  
a b c d

a : Manufacturing Year -- Last digit of the western calendar year

b : Manufacturing Month -- shown by 1 digit as below

Jan. ... A	Jul. ... G
Feb. ... B	Aug. ... H
Mar. ... C	Sep. ... I
Apr. ... D	Oct. ... J
May ... E	Nov. ... K
Jun. ... F	Dec. ... L

c : Serial No. (Maximum 6 digits)

d : Model Identification

FLxxxx ... TBD

### 2) Label Color

TBD

### 3) Labeling Position : Refer to the following figure.

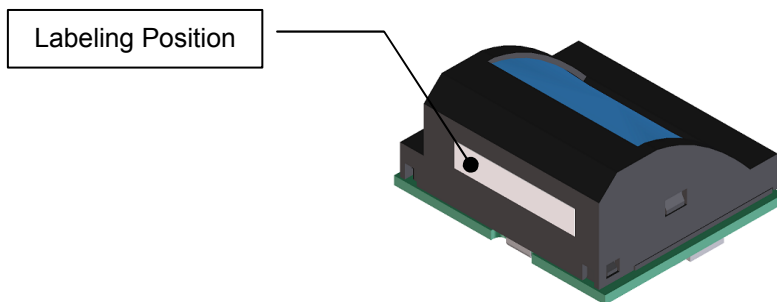


Fig. 13. Labeling Position