1.3 cm (Type 0.5) Active Matrix Color OLED Panel

# OL51D

## Description

The OL51D is a 1.3 cm (type 0.5) diagonal, 1024 × 768 dots active matrix color OLED panel module using single crystal silicon transistors. This panel incorporates panel driver and logic driver, and realizes small size, light weight and high definition. It enables full color display in NTSC/PAL progressive system.

(Applications: View finders, head mounted displays, very small monitors etc.)

## Features

- Small size high definition type 0.5 display  dots: 1024 (RGB)×768 = 2.36 M dots
- High contrast
- Wide color reproduction range
- High-speed response
- Thin type and light weight
- Power saving function
- Up/down and/or right/left inverse display function
- Orbit supported

## Element Structure

Active matrix color OLED display element with on-chip driver using single crystal silicon transistors

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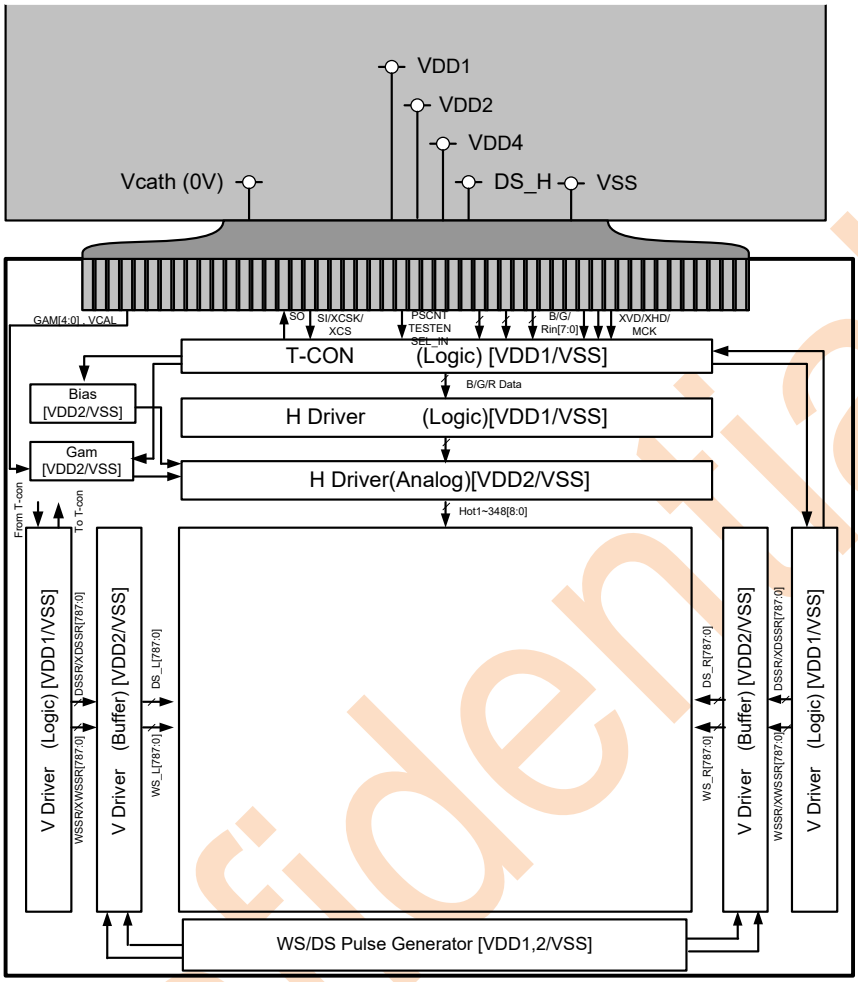
## Block Diagram

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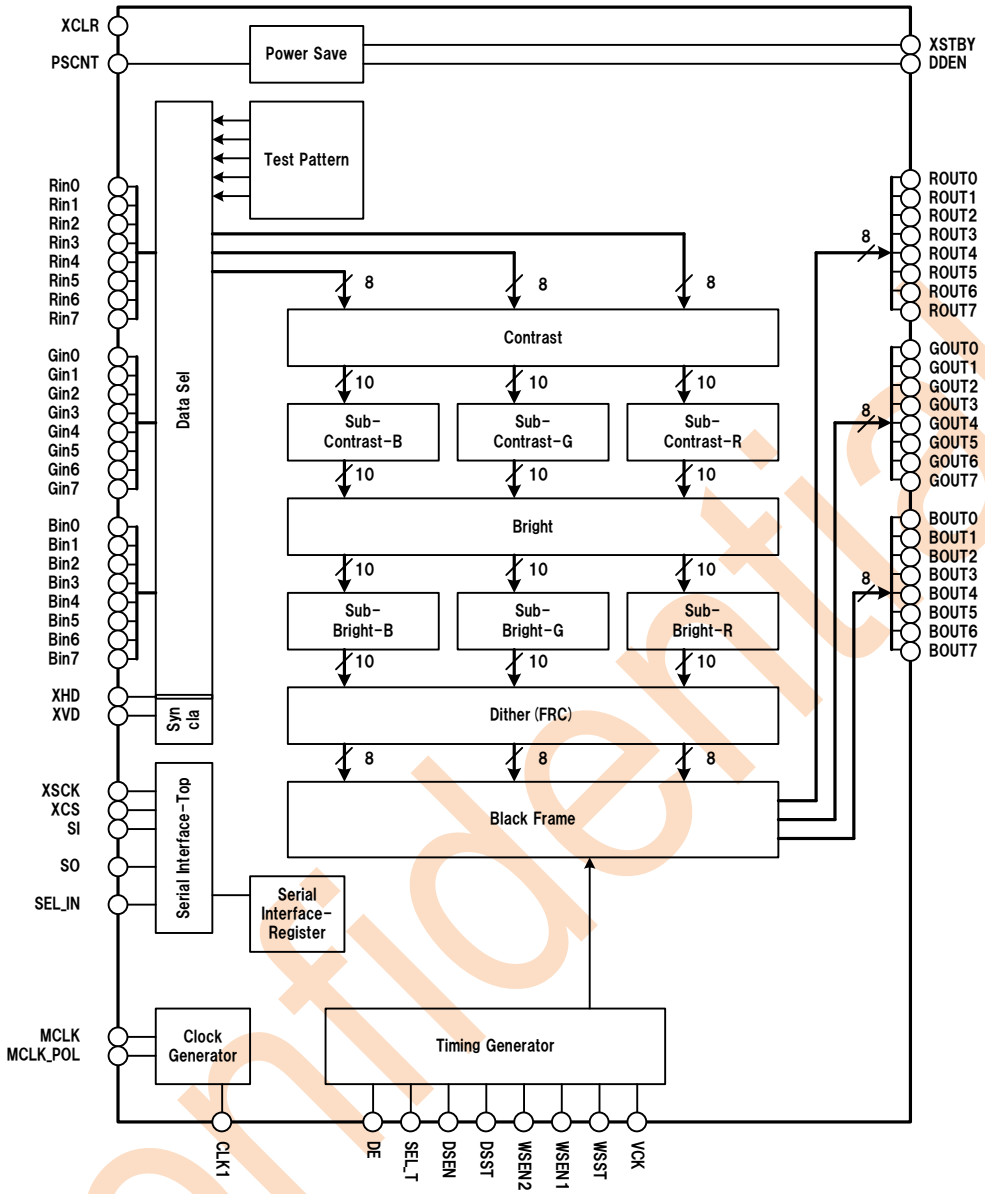
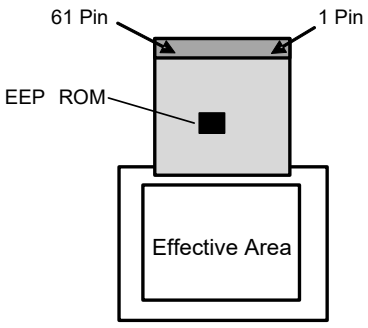
## T-CON Block Diagram




## Pin Assignment




### EEP ROM

This panel has an EEP ROM on the flexible connector.

This EEP ROM stores the register setting values used to adjust the luminance and white chromaticity.

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## Pin Description

| Pin No. (FPC side) | Symbol | Type | Description | Equivalent circuit |
|---|---|---|---|---|
| 1 | VSS | Power supply | GND | |
| 2 | VDD4 | Power supply | 10V power supply | |
| 3 | DS_H | Power supply | DS-High power supply | |
| 4 | VDD2 | Power supply | DAC input stage, Data input level shifter<br>DAC selector, Output selector<br>Gamma generation, V driver<br>Amplifier output stage power supply | |
| 5 | | | | |
| 6 | Vcath | Power supply | EL cathode power supply | |
| 7 | VSS | Power supply | GND | |
| 8 | VDD 1 | Power supply | 3 V power supply | |
| 9 | MCLK | Input | Clock | *1 |
| 10 | XHD | Input | Horizontal sync signal | *1 |
| 11 | XVD | Input | Vertical sync signal | *1 |
| 12 | XCLR | Input | System reset | *2 |
| 13 | Rin7 | Input | Digital R signal | *1 |
| 14 | Rin6 | Input | Digital R signal | *1 |
| 15 | Rin5 | Input | Digital R signal | *1 |
| 16 | Rin4 | Input | Digital R signal | *1 |
| 17 | Rin3 | Input | Digital R signal | *1 |
| 18 | Rin2 | Input | Digital R signal | *1 |
| 19 | Rin1 | Input | Digital R signal | *1 |
| 20 | Rin0 | Input | Digital R signal | *1 |
| 21 | Gin7 | Input | Digital G signal | *1 |
| 22 | Gin6 | Input | Digital G signal | *1 |
| 23 | Gin5 | Input | Digital G signal | *1 |
| 24 | Gin4 | Input | Digital G signal | *1 |
| 25 | Gin3 | Input | Digital G signal | *1 |
| 26 | Gin2 | Input | Digital G signal | *1 |
| 27 | Gin1 | Input | Digital G signal | *1 |
| 28 | Gin0 | Input | Digital G signal | *1 |
| 29 | VDD 1 | Power supply | 3 V power supply | |
| 30 | VSS | Power supply | GND | |
| 31 | Bin7 | Input | Digital B signal | *1 |
| 32 | Bin6 | Input | Digital B signal | *1 |
| 33 | Bin5 | Input | Digital B signal | *1 |
| 34 | Bin4 | Input | Digital B signal | *1 |
| 35 | Bin3 | Input | Digital B signal | *1 |
| 36 | Bin2 | Input | Digital B signal | *1 |
| 37 | Bin1 | Input | Digital B signal | *1 |
| 38 | Bin0 | Input | Digital B signal | *1 |
| 39 | XSCAN_MODE | Input | Serial communication mode<br>Low: MSB First<br>High: LSB First | *2 |
| 40 | E2PROM_XCS | Input | Serial communication chip select for EEP ROM | *2 |
| 41 | E2PROM_WP | Input | Serial communication data write control signal for EEP ROM | *2 |
| 42 | XCS | Input | Serial communication<br>Chip select | *2 |
| 43 | XSCK | Input | Serial communication<br>Serial clock (shared with EEP ROM XSCK) | *2 |

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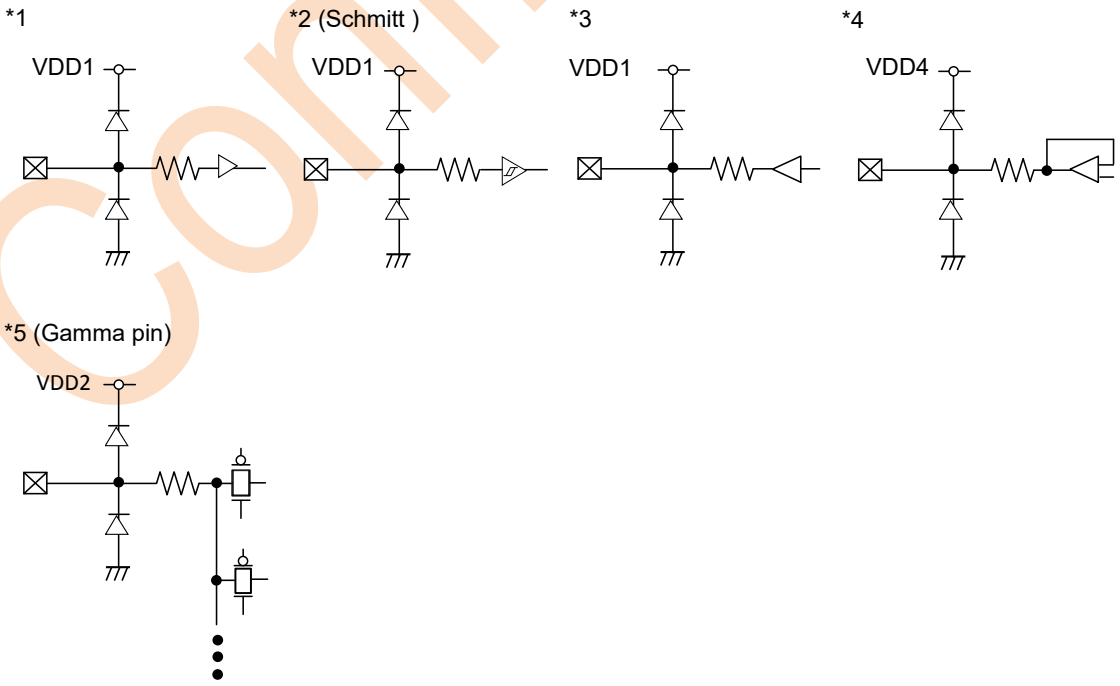
| Pin No. (FPC side) | Symbol | Type | Description | Equivalent circuit |
|---|---|---|---|---|
| 44 | SI | Input | Serial communication<br>Input data (shared with EEP ROM SI) | *2 |
| 45 | E2PROM_SO | Output | SO for EEP ROM<br>Serial communication<br>Output data | *3 |
| 46 | SO | Output | Panel SO<br>Serial communication<br>Output data | *3 |
| 47 | VDD 1 | Power supply | 3 V power supply | |
| 48 | VSS | Power supply | GND | |
| 49 | VCAL | Output | Correction voltage output in temperature compensation circuit | *4 |
| 50 | VGAM 4 | Output | Gamma top reference voltage (255) | *5 |
| 51 | VGAM 3 | Output | Gamma reference voltage (128) | *5 |
| 52 | VGAM 2 | Output | Gamma reference voltage (32) | *5 |
| 53 | VGAM1 | Output | Gamma bottom reference voltage (1) | *5 |
| 54 | VGAM0 | Output | Vofs voltage (0) | *5 |
| 55 | VSS | Power supply | GND | |
| 56 | Vcath | Power supply | EL cathode power supply | |
| 57<br>58 | VDD 2 | Power supply | DAC input stage, Data input level shifter<br>DAC selector, Output selector<br>Gamma generation, V driver<br>Amplifier output stage power supply | |
| 59 | DS_H | Power supply | DS-High power supply | |
| 60 | VDD4 | Power supply | 10V power supply | |
| 61 | VSS | Power supply | GND | |

## Equivalent Circuit

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## Absolute Maximum Ratings

| Item | Symbol | Min. | Maximum Ratings | Unit |
|---|---|---|---|---|
| 3 V power supply | VDD1 | -0.3 | 4.0 | V |
| 12.5 V power supply | VDD2 | -0.3 | 18.5 | V |
| 10 V power supply | VDD4 | -0.3 | 10.3 | V |
| DS-High power supply | DS_H | -0.3 | VDD2 | V |
| EL cathode voltage | Vcath | -0.3 | VDD2 | V |
| Logic input voltage | Vi | -0.3 | VDD1+（0.3） | V |
| Storage temperature | Tpnl | -30 | +80 | °C |

## Recommended Operating Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| 3 V power supply | VDD1 | 2.7 | 3.0 | 3.3 | V |
| 12.5 V power supply | VDD2 | 12.0 | 12.5 | 13.0 | V |
| 10 V power supply | VDD4 | 9.7 | 10.0 | 10.3 | V |
| DS-High power supply | DS_H | 12.0 | 12.5 | 13.0 | V |
| EL cathode voltage | Vcath | -0.3 | 0 | 0.3 | V |
| Clock frequency | fCLK | | 54.0 | 54.5 | MHz |
| Operating temperature range | Tpnl | -10 | | 70 | °C |

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## Electrical Characteristics

### 1. DC Characteristics

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-level input voltage | VIH | | 0.7VDD1 | | VDD1 | V |
| Low-level input voltage | VIL | | 0 | | 0.3VDD1 | V |
| High-level input voltage | Vt+ | Schmitt input | 0.7VDD1 | | VDD1 | V |
| Low-level input voltage | Vt- | Schmitt input | 0 | | 0.3VDD1 | V |
| Vt+ - Vt- | Vhys | Schmitt input | | 0.50 | | V |
| Logic High -level Output voltage | VOH | | VDD1-0.4 | | | V |
| Logic Low -level Output voltage | VOL | | | | 0.4 | V |

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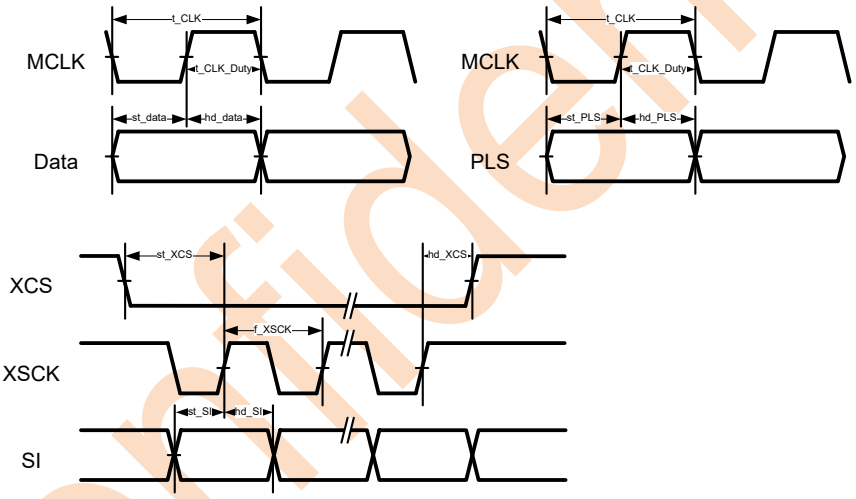
## 2. AC Characteristics

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse cycle | t_CLK | | 15.3 | 18.5 | | ns |
| Clock duty | t_CLK_duty | All mode (54 MHz/40.5 MHz/32.4 MHz) common | 40 | 50 | 60 | % |
| Data setup time | st_Data | Vi = 2.7 to 3.6 V | 2.5 | | | ns |
| Data hold time | hd_Data | Vi = 2.7 to 3.6 V | 1.8 | | | ns |
| Control pulse setup time | st_PLS | Vi = 2.7 to 3.6 V | 2.5 | | | ns |
| Control pulse hold time | hd_PLS | Vi = 2.7 to 3.6 V | 1.8 | | | ns |
| XSCK frequency | f_SCLK | | | 0.8 | 2.5 | MHz |
| XCS setup time | st_XCS | | 0.4 | | | µs |
| XCS hold time | hd_XCS | | 0.2 | | | µs |
| SI setup time | st_SI | | 0.2 | | | µs |
| SI hold time | hd_SI | | 0.2 | | | µs |




## 3. Power Consumption

| Item | Symbol | Condition | Typ. (*) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | 500 | 300 | 200 | 120 | Standby | cd/m$^2$ |
| VDD1 power consumption | PDD1 | Tpnl = 40℃ | 43 | | | | 0 | mW |
| VDD2 power consumption | PDD2 | | 107 | | | | 3.3 | mW |
| VDD4 power consumption | PDD4 | | 0 | | | | 0 | mW |
| DS-High power consumption | PDS_H | | 330 | 195 | 130 | 75 | 0 | mW |
| Total | PTTL | | 480 | 345 | 280 | 225 | 3.3 | mW |

*All white raster, Frame rate=60Hz, Clock=54MHz

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## Optical Characteristics

### 1. Optical Characteristics

| Item | | Symbol | System | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Luminance | Mode 2 | L2 | 1 | 102 | 120 | 138 | $Cd/m^2$ |
| | Mode 0 | L0 | 1 | 170 | 200 | 230 | $Cd/m^2$ |
| | Mode 3 | L3 | 1 | 255 | 300 | 345 | $Cd/m^2$ |
| | Mode 4 | L4 | 1 | 400 | 500 | 600 | $Cd/m^2$ |
| Contrast | | CR | 1 | 5,000 | — | — | |
| Chromaticity | W (Mode 0,2&3) | x | 1 | 0.298 | 0.310 | 0.322 | CIE |
| | | y | 1 | 0.298 | 0.310 | 0.322 | CIE |
| | W (Mode 4) | x | 1 | 0.295 | 0.310 | 0.325 | CIE |
| | | y | 1 | 0.295 | 0.310 | 0.325 | CIE |
| | R | x | 1 | 0.635 | 0.655 | 0.675 | CIE |
| | | y | 1 | 0.310 | 0.330 | 0.350 | CIE |
| | G | x | 1 | 0.255 | 0.275 | 0.295 | CIE |
| | | y | 1 | 0.625 | 0.645 | 0.665 | CIE |
| | B | x | 1 | 0.127 | 0.147 | 0.167 | CIE |
| | | y | 1 | 0.045 | 0.065 | 0.085 | CIE |

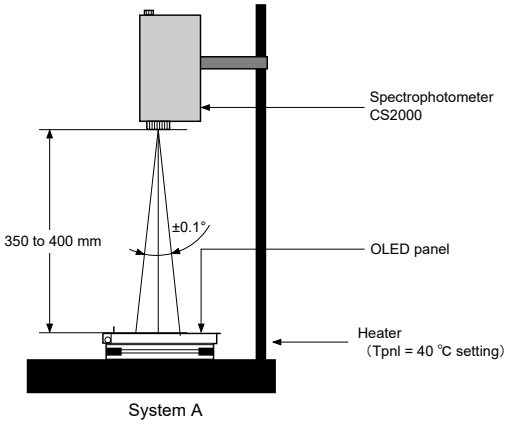
Drive conditions : EEP-ROM register setting
Measurement temperature : Tpnl = 40 ˚C
Measurement point : One point on the screen center

### 2. Measurement method and system 1

All white display : All RGB signal data is set to High.
All black display : All RGB signal data is set to Low.

◆Luminance, color temperature and Chromaticity:
Measured in Measurement System A.

◆Contrast:
Measure the luminance of the panel in Measurement System A and substitute them in the formula below.
Contrast = Luminance in all white display / Luminance in all black display



System A

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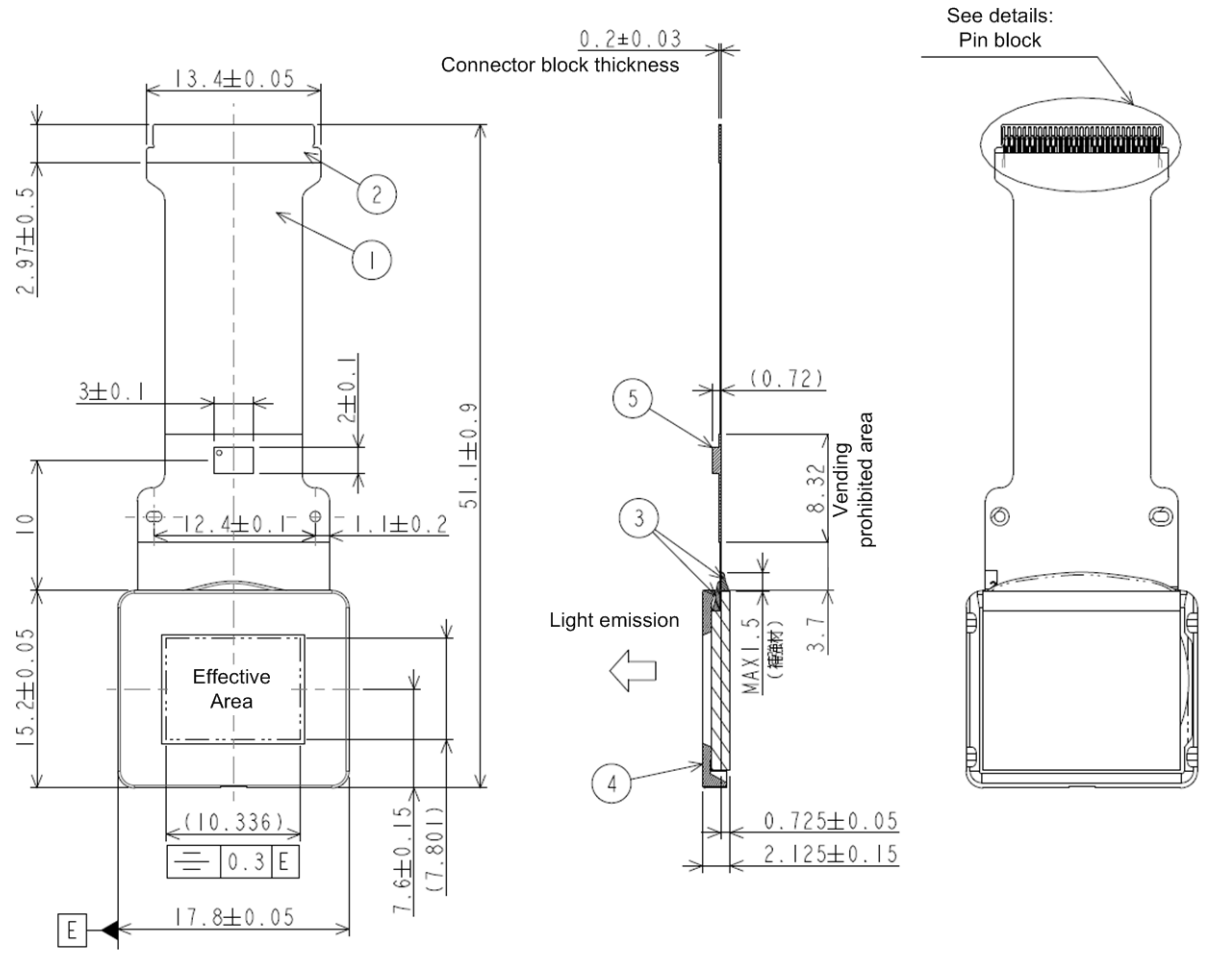
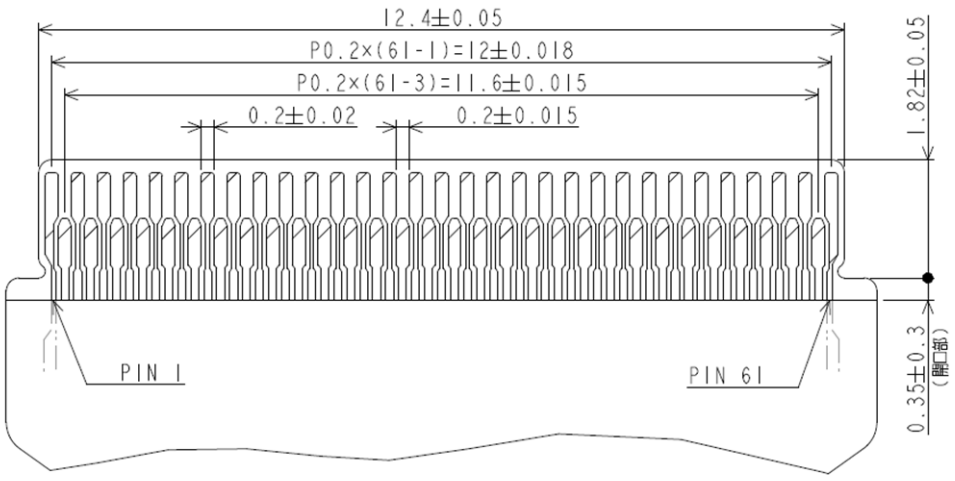
## Package Outline

(Unit : mm)




Details of pin block

| No | Items |
|---|---|
| 1 | FPC |
| 2 | Reinforcing Plate |
| 3 | Stiffener |
| 4 | Frame |
| 5 | ROM |

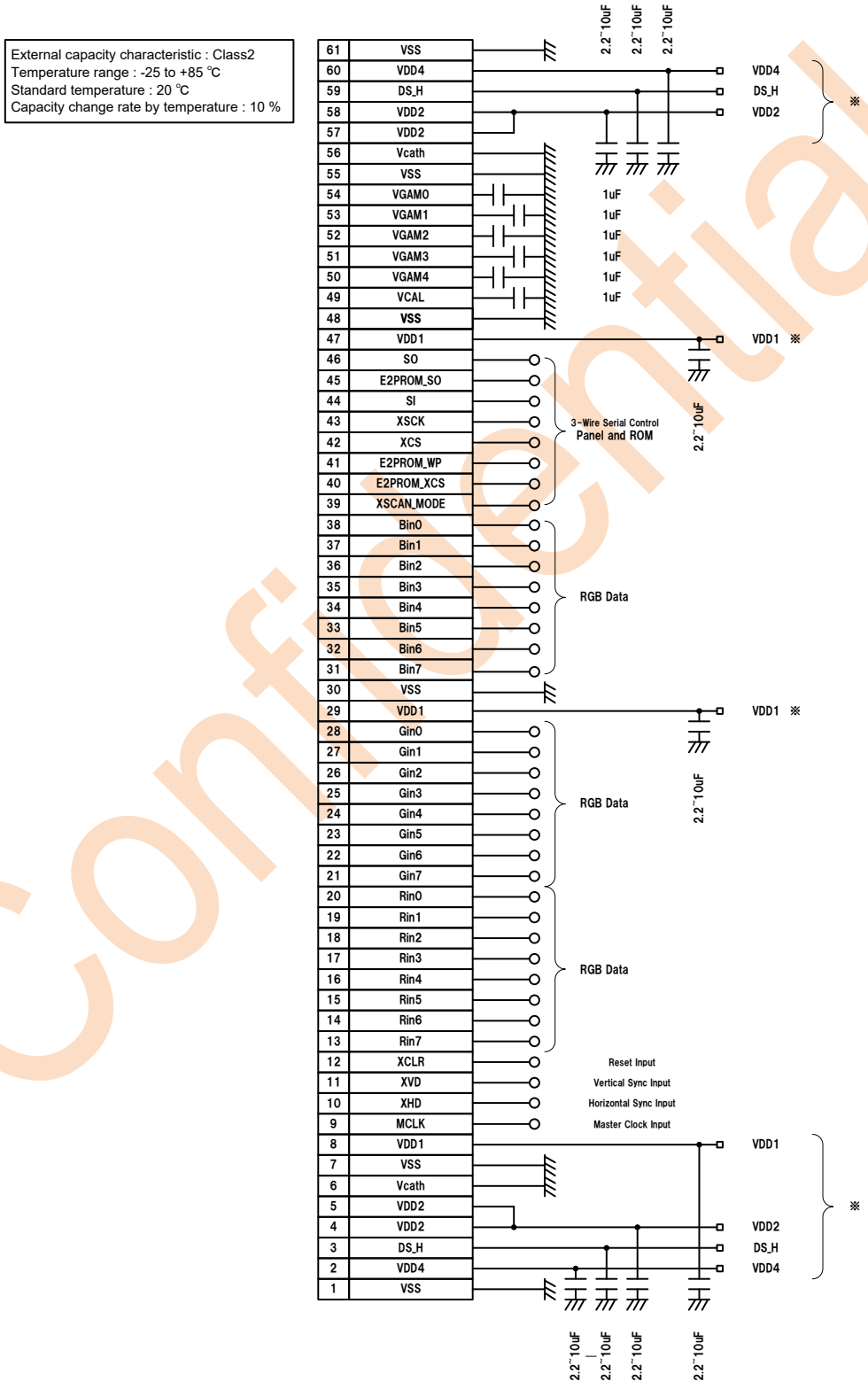
Weight: 1.0g

## Recommendation

### 1. Peripheral circuits

Reccommended periheral circuits of panel pin is as follows.

*2.2μF to 10μF capacitor needs to be mounted for each power supply (※). Short capacitance may affect the picture quality.

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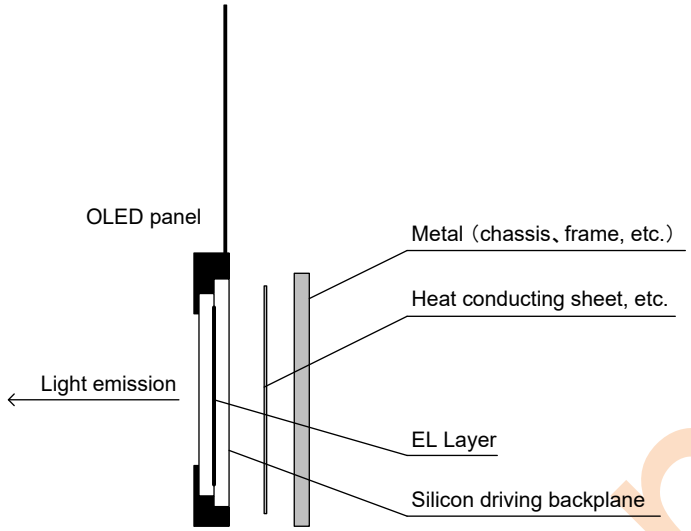
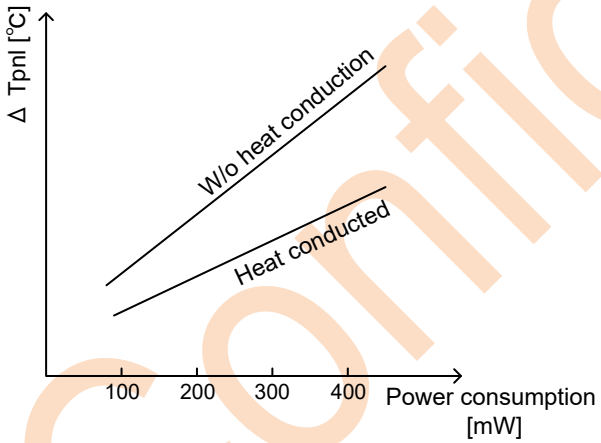
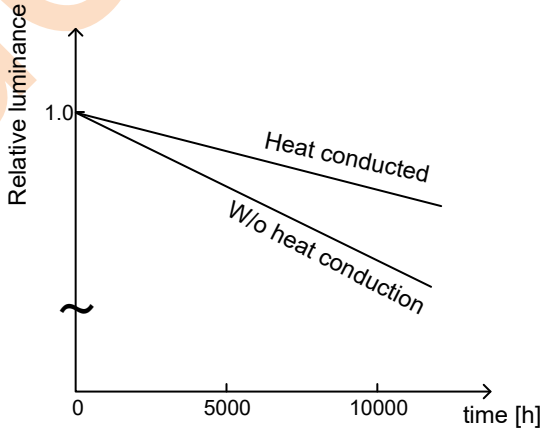
## 2. Panel Temperature Control by Heat Condcution

The tempareture of OLED panel rises dut to power consumption of EL layer and silicon driving backplane. Higher panel temperature may affects the luminance degradation in the long span.

To control the panel temperature , heat conduction between panel back side(silicon bakplane) and metal (chassis, frame,etc.) is recommended.

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## Notes on Handling

1. Static charge prevention

   Be sure to take the following protective measures. OLED panels (modules) are easily damaged by static charges.

   (1) Use non-chargeable gloves, use bare hands.
   (2) Use a wrist strap when handling.
   (3) Do not touch any electrodes of the panel.
   (4) Wear non-chargeable clothes and conductive shoes.
   (5) Install grounded conductive mats on the working floor and working table.
   (6) Keep the panel (module) away from any charged materials.

2. Protection from dust and dirt

   (1) Operate in a clean environment.
   (2) Do not touch the panel (module) surface. The surface is easily scratched.
   When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   (3) Apply ionized air blow or air blow to the panel when dust and dirt fall on the panel surface.

3. Others

   (1) Do not hold the flexible board or twist or bend it because the flexible board connection block is easily affected by twist.
   (2) The minimum fold radius of the flexible board is 1 mm.
   (3) Do not drop the panel.
   (4) Do not twist or bend the panel.
   (5) Keep the panel away from heat sources.
   (6) Do not dampen the panel with water or other solvents.
   (7) Do not store or use of the panel at high temperatures or high humidity, as this may affect the characteristics.
   (8) When disposing this panel, handle it as an industrial waste complying with related regulations.
   (9) Do not store or use the panel in reactive chemical substances (including alcohol) environment, as this may affect the performance.
   (10) This panel is delivered with packed in the degassed aluminum laminated bag.
   When storing this panel after unsealing bags, put it into the aluminum laminated bag again and seal it with tapes with the opening folded after entering desiccants.

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