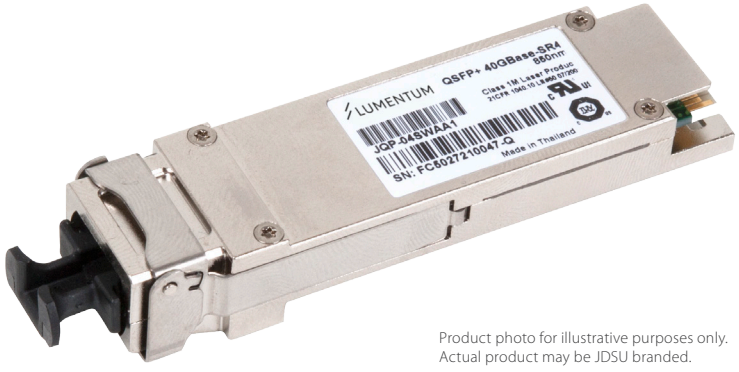
LUMENTUM

QSFP+ 40 G SR4 Optical Transceiver – 850 nm for up to 100 m Reach

JQP Series



Product photo for illustrative purposes only.
Actual product may be JDSU branded.

The Lumentum 40 G QSFP+ Optical Transceiver is a parallel photonic-integrated fiberoptic transceiver that provides a high-speed link at a signaling rate of 41.25 Gbpsover 100 m of OM3 multimode optical fiber. The module complies with the QSFP+MSA SFF-8436 and with IEEE802.3-2012 Clause 86 and Annex 86A.

The transceiver integrates the receive and transmit path on one module. In the transmit side, four 10.3125 Gbps serial data streams are passed to an array of four laser drivers. The laser driver array controls an array of four vertical cavity surface emitting lasers (VCSELs) at a wavelength of 850 nm; the optical output of the VCSELs enable data transmission over a multimode ribbon-fiber array through an industry-standard MPO connector. In the receive side, the four 10.3125 Gbps optical data streams from the MPO connector are recovered through an array of four PIN photodetectors and then passed to an array of four transimpedance amplifiers, and passed out to the 38-way edge connector. This module has an option to operate with four independent 10 G transceivers through a MPO-to-LC break out cable. This module features a hot-pluggable electrical interface, low power consumption, and a 2-wire management interface.

Key Features

- Supports 40 Gigabit Ethernet and 4 x 10G Base-SR compatible fanout applications
- Integrated transmitter and receiver
- MPO optical receptacle
- RoHS 6/6 compliant
- Operating case temperature range from –5 to 70°C
- Low power consumption (<1.5 W max)
- Hot-pluggable to 38-pin electrical interface
- 2-wire management interface

Applications

- Wide area networks (WAN)
- Local area networks (LAN)
- Storage area networks (SAN)
- 40 G Ethernet switches

Compliance

- IEEE802.3-2012, Clause 86, 40GBase-SR4
- Electrical interface: IEEE802.3-2012 Annex 86A, XLPPI
- QSFP+ MSA SFF-8436 Rev. 4.7
- Class 1M laser safety
- Tested in accordance with Telcordia GR-468

Section 1 Functional Description

The transceiver includes parallel electric and optical devices with both transmit and receive functions contained in a single module. It is designed to be compliant with IEEE 802.3-2012 Clause 86 40GBase-SR4 over 100 m of OM3 multimode fiber at an aggregated signaling rate of 41.25 Gbps. This module has an option to operate with four independent 10GBase-SR, IEEE 802.3 Clause 52 compatible 10 G transceivers through an MPO-to-LC breakout cable (compliant at 100 m over 50 µm OM3 fiber). The transceiver is also fully compliant with the QSFP+ MSA specification SFF-8436 Rev. 4.7. A block diagram is shown in Figure 1.

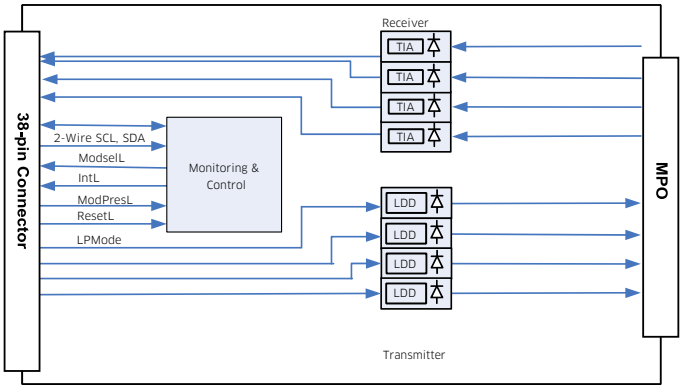


Figure 1. Functional block diagram

1.1 Transmitter

The transmitter path converts four lanes of serial NRZ electrical data at a line rate of 10.3125 Gbps to standard compliant optical signals. The transmitter accepts a 100 Ω differential 190 mV peak-to-peak to 700 mV peak-to-peak 10 Gbps CML electrical signal on TXnp and TXnn pins.

The transmitter inputs are connected to an array of four laser drivers, which transform the small swing digital voltage to an output modulation that drives an array of four VCSEL. The optical output signals from the four VCSELs are coupled into four multimode fibers through an industry-standard female MPO connector. Closed-loop control of the transmitted power and modulation swing over temperature and voltage variations is provided.

1.2 Receiver

The receiver converts the incoming four lanes of NRZ optical data through an industry-standard MPO connector into an array of four PIN photodetectors. The photo current from the PIN photodetector is converted to a voltage in a high-gain transimpedance amplifier.

The amplified signals are passed to the RXnp and RXnn pins as a 100 Ω 300 mV peak-to-peak to 800 mV peak-to-peak CML signal. The output signal meets the IEEE802.3-2012 Annex 86A XLPPI requirements.

1.3 Low-Speed Signaling

The transceiver has several low-speed interface connections plus a 2-wire serial interface (SCL and SDA). These connections include; Low Power Mode (LPMode), Module Select (ModSelL), Interrupt (IntL), Module Present (ModPrsL) and Reset (ResetL) as shown in Figure 1.

ModSelL – The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "high," the module does not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

ResetL – The ResetL pin is pulled up to V_{CC} inside the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts upon the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init), the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion), the module will post this completion of reset interrupt without requiring a reset.

LPMode – The LPMode pin is pulled up to V_{CC} inside the QSFP+ module. The QSFP+ SR4 module does not use the LPMode function.

ModPrsL – ModPrsL is pulled up to V_{CC} Host on the host board and grounded in the module. The ModPrsL is asserted "low" when the module is inserted and deasserted "high" when the module is physically absent from the host connector.

IntL – IntL is an output pin. When "low," it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

Section 2 Application Schematics

Recommended MSA connections to the transceiver are shown in Figure 2.

Power supply filtering is recommended for the transceiver. Power-supply noise including ripple should be no more than 50 mV from 1 kHz to frequency of operation, measured at V_{CC} Host.

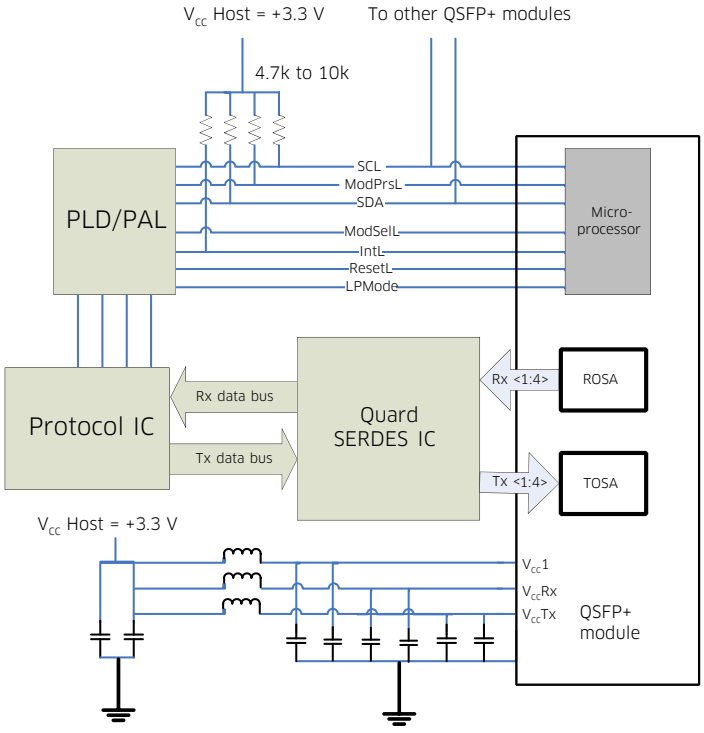


Figure 2. Application schematics

Section 3 Specifications

Technical specifications include:

Section 3.1	Absolute Maximum Ratings
Section 3.2	Operating Conditions
Section 3.3	Electrical Pin Function Definitions
Section 3.4	QSFP+ XLPPI Reference Model Compliance Points
Section 3.5	Electrical Characteristics
Section 3.6	Jitter and Eye-Mask Specifications
Section 3.7	Timing Requirement of Control and Status I/O
Section 3.8	QSFP+ 2-wire Interface Protocol and Management Interface
Section 3.9	Optical Transmitter Characteristics
Section 3.10	Optical Receiver Characteristics
Section 3.11	Regulatory Compliance
Section 3.12	PCB Layout
Section 3.13	Module Outline
Section 3.14	Connectors

3.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage temperature	T_{ST}	–40 to +85	°C
Operating case temperature	T_{OP}	–5 to +70	°C
Relative humidity	RH	5 to 85 (noncondensing)	%
Static electrical discharge (high speed) (human body model)	ESD	1000	V
Power supply voltages	$V_{CC}3$, max	–0.3 to 3.63	V
Receive input optical power (damage threshold)	P_{rdt}, min	3.4	dBm

Note:
Absolute maximum ratings represent the damage threshold of the device. Damage may occur if the device is operated above the limits stated here except for brief excursions. Performance is not guaranteed and reliability is not implied for operation at any condition outside the recommended operating limits.

3.2 Operating Conditions

Part Number	40 GE (40GBase-SR4)	40 GE Fanout (4x10G Base-SR compatible)	Operating Case Temperature (–5 to 70°C)
JQP-04SWAAx	X		X
JQP-04SRABx	X	X	X

Note:
Performance is not guaranteed and reliability is not implied for operation at any condition outside the recommended operating limits.

3.3 Electrical Pin Function Definitions

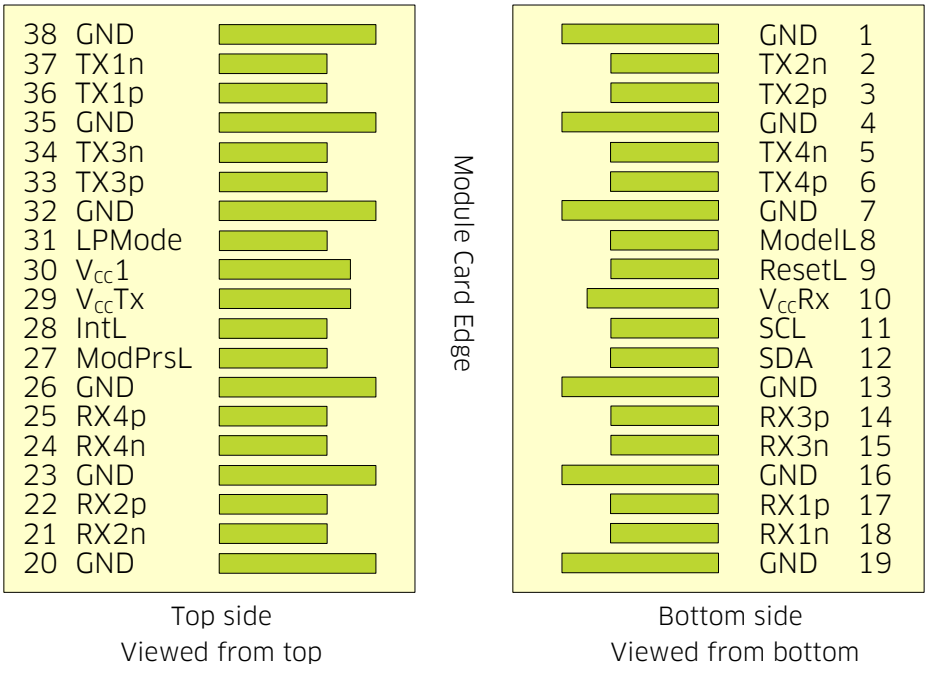


Figure 3. Module pin pad layout

Electrical Pin Descriptions

Pin Number	Type	Name	Description
1		GND	Module ground
2	CML-I	Tx2n	Transmitter inverted data input
3	CML-I	Tx2p	Transmitter non-inverted data input
4		GND	Module ground
5	CML-I	Tx4n	Transmitter inverted data input
6	CML-I	Tx4p	Transmitter non-inverted data input
7		GND	Module ground
8	LVTTL-I	ModSelL	Module select
9	LVTTL-I	ResetL	Module reset
10		V_{CC}Rx	+3.3 V power supply receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Module ground
14	CML-O	Rx3p	Receiver non-inverted data output
15	CML-O	Rx3n	Receiver inverted data output
16		GND	Module ground
17	CML-O	Rx1p	Receiver non-inverted data output
18	CML-O	Rx1n	Receiver inverted data output
19		GND	Module ground
20		GND	Module ground
21	CML-O	Rx2n	Receiver non-inverted data output
22	CML-O	Rx2p	Receiver inverted data output
23		GND	Module ground
24	CML-O	Rx4n	Receiver non-inverted data output
25	CML-O	Rx4p	Receiver inverted data output
26		GND	Module ground
27	LVTTL-O	ModPrsL	Module present
28	LVTTL-O	IntL	Interrupt
29		V_{CC}Tx	+3.3 V power supply transmitter
30		V_{CC}1	+3.3 V power supply
31	LVTTL-I	LPMode	Low-power mode (no effect)
32		GND	Module ground
33	CML-I	Tx3p	Transmitter non-inverted data output
34	CML-I	Tx3n	Transmitter inverted data output
35		GND	Module ground
36	CML-I	Tx1p	Transmitter non-inverted data output
37	CML-I	Tx1n	Transmitter inverted data output
38		GND	Module ground

3.4 QSFP+ XLPPI Reference Model Compliance Points

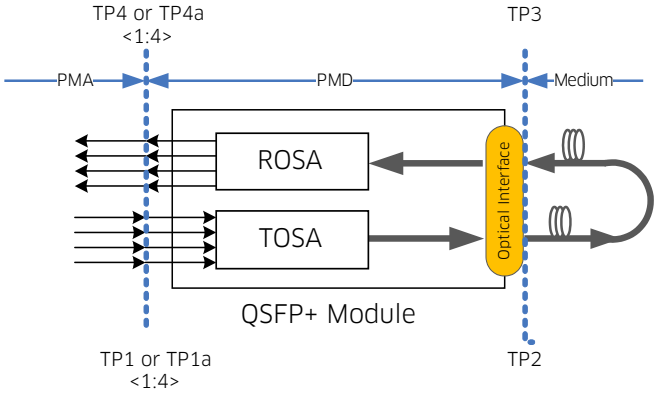


Figure 4. Transmitter and receiver reference points

Table 1. Test Point Directions

Test Point	Direction
TP1	Looking downstream into PMD transmitter input
TP1a	Looking upstream into PMA transmitter output
TP2	Looking upstream into optical transmitter output
TP3	Looking upstream into medium output
TP4	Looking upstream into PMD receiver output
TP4a	Looking downstream into PMA receiver input

3.5 Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Supply Currents and Voltages						
Voltage	$V_{CC}3$	3.13	3.3	3.47	V	With respect to GND
Supply Current	$I_{CC}3$			432	mA	
Power dissipation	Pwr			1.5	W	
Low-Speed Control and Sense Signals (detailed specification in SFF-8436 Rev 3.8)						
Outputs (Interrupt, ModPrsL)	V_{OL}	0		0.4	V	R_{pullup} pulled to host _V_{CC}, measured at host side of connector
						I_{OL}(max) = 2 mA
	V_{OH}	host_V_{CC} – 0.5		host_V_{CC} + 0.3	V	R_{pullup} pulled to host _V_{CC}, measured at host side of connector
Inputs (ModSelL, ResetL, LPMode)	V_{IL}	–0.3		0.8	V	Pulled up in module to $V_{CC}3$
	V_{IH}	2		$V_{CC}3$ + 0.3	V	Pulled up in module to $V_{CC}3$
SCL and SDA inputs	V_{IL}	–0.3		$V_{CC}3$ * 0.3	V	R_{pullup} pulled to host _V_{CC}, measured at QSFP+ side of connector
	V_{IH}	$V_{CC}3$ * 0.7		$V_{CC}3$ + 0.5	V	R_{pullup} pulled to host _V_{CC}, measured at QSFP+ side of connector
Transmitter Inputs per Lane (detailed specification in IEEE802.3ba Annex 86A)						
Data input baud rate nominal			10.3125		Gbps	
Data input bit rate tolerance		–100		+100	ppm	TP1 and TP1a
Data input differential impedance	R_I	90	100	110	Ω	
Tx input equalizer	Tx EQ	0	2	4	Inches	Tx EQ optimized for ~2 inches of host PCB. Performance may degrade if host board is > 4 inches of uncompensated PCB traces.
Receiver Outputs per Lane (detailed specification in IEEE802.3ba Annex 86A)						
Data output baud rate nominal			10.3125		Gbps	
Data output bit rate tolerance		–100		+100	ppm	TP4

3.6 Jitter and Eye-Mask Specifications

Parameter	Test Point	Minimum	Typical	Maximum	Unit	Notes
Electrical Interface and Jitter Specifications						
Differential input return loss	TP1	See 86A.4.1.1			dB	10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10		—	dB	10 MHz to 11.1 GHz
Single-ended output voltage tolerance	TP4	–0.3		4	V	Referred to signal common
AC common-mode output voltage (RMS)	TP4	—		7.5	mV	
Termination mismatch at 1 MHz	TP4	—		5	%	
Differential output return loss	TP4	See 86A.4.2.1		—	dB	10 MHz to 11.1 GHz
Common-mode output return loss	TP4	See 86A.4.2.1		—	dB	10 MHz to 11.1 GHz
Output transition time, 20% to 80%	TP4	28		—	ps	
J2 jitter output	TP4	—		0.42	UI	
J9 jitter output	TP4	—		0.65	UI	
Eye-Mask Specification						
Eye mask coordinates X1, X2 Y1, Y2	 TP1a TP1a	 0.11 95		 0.31 350	 UI mV	 Hit ratio: $5x10^{-5}$
Crosstalk source VMA, each lane	TP1a		700		mV	
Crosstalk source transition times, 20 to 80%	TP1a		37		pps	
Eye mask coordinates X1, X2 Y1, Y2	 TP4 TP4	 0.29 150		 0.5 425	 UI mV	 Hit ratio: $5x10^{-5}$
Crosstalk calibration signal VMA	TP4		850		mV	
Crosstalk calibration signal transition times, 20% to 80%	TP4		34		ps	While calibrating compliance signal

3.7 Timing for Soft Control and Status Functions

Parameter	Symbol	Maximum	Unit	Conditions
Initialization time	t_init	2000	ms	Time from power on, hot plug or rising edge of reset until the module is fully functional. This time does not apply to non-power level 0 modules in low power state.
Reset init assert time	t_reset_ini	2	µs	A reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin[1].
Serial bus hardware ready time	t_serial	2000	ms	Time from power on until the module responds to data transmission over the 2-wire serial bus.
Monitor data ready time	t_data	2000	ms	Time from power on to data not ready, bit 0 of Byte 2, de-asserted and IntL asserted.
Reset assert time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional.
IntL assert time	t_{on}_IntL	200	ms	Time from occurrence of condition triggering IntL until V_{out}:IntL=V_{OL}.
IntL de-assert time	t_{off}_IntL	500	µs	Time from clear on read operation of associated flag until V_{out}:IntL=V_{OH}. This includes de-assert times for Rx LOS, Tx Fault, and other flag bits.
Rx LOS assert time	t_{on}_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx fault assert time	t_{on}_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted.
Flag assert time	t_{on}_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask assert time	t_{on}_mask	100	ms	Time from mask bit set (value = 1b) until associated IntL assertion is inhibited.
Mask de-assert time	t_{off}_mask	100	ms	Time from mask bit set (value = 0b) until associated IntL operation resumes.

1. If the host and the module are in the middle of a 2-wire interface communication with a reset pulse present, the minimum reset pulse time can be up to 5 µs.

3.8 2-Wire Interface Protocol and Management Interface

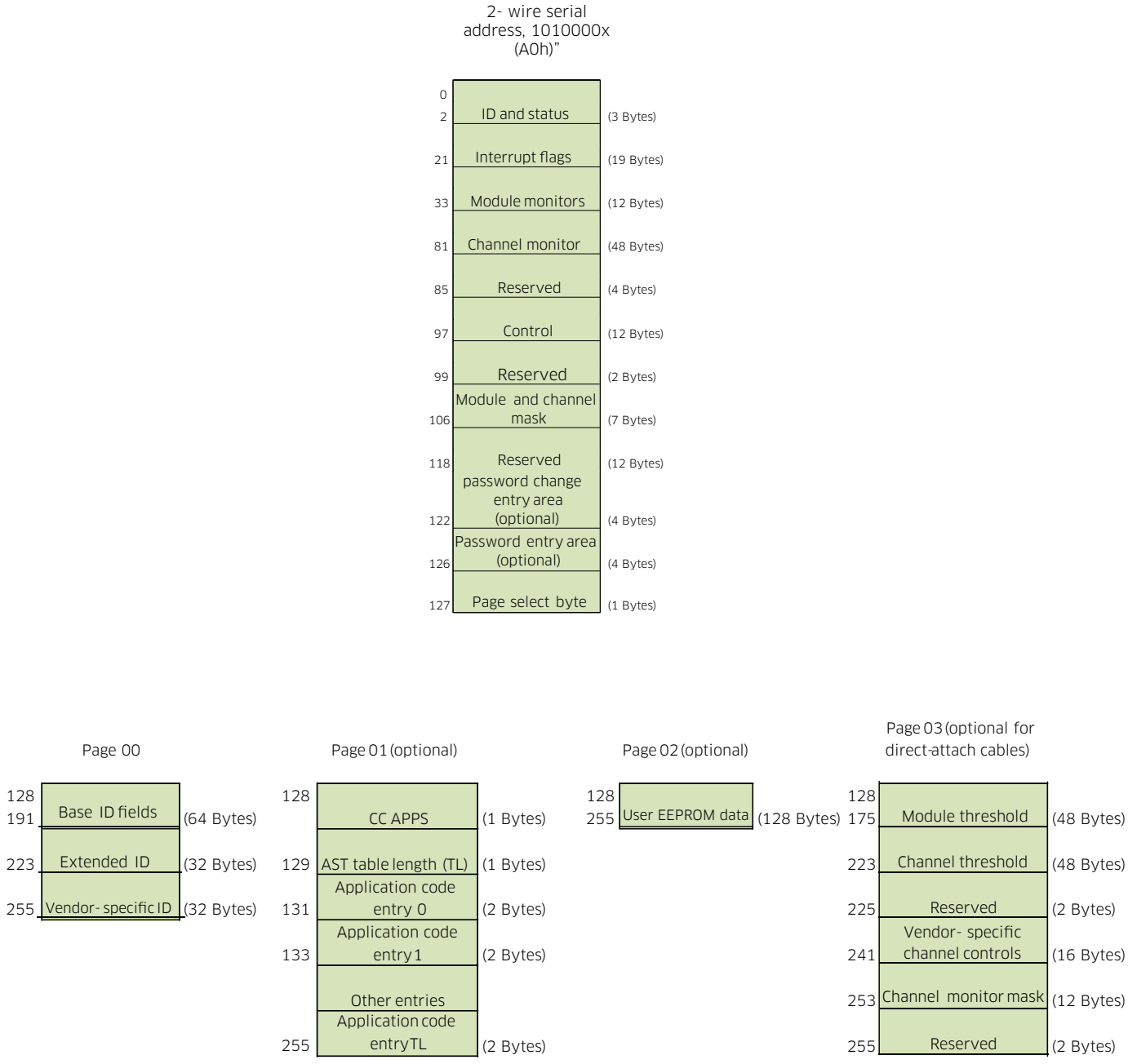


Figure 5. Memory map

3.9 Optical Transmitter Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling rate, each lane			10.3125		Gbps
Center wavelengths	λ	840		860	nm
RMA spectral width 40GBase-SR4 4x10G Base-SR compatible fanout	 RMS RMS			 0.65 0.45	 nm nm
Average launch power, each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 AOP AOP	 –7.6 –8		 2.4 –1	 dBm dBm
Optical modulation amplitude, each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 OMA OMA	 –5.6 –3.9		 3	 dBm dBm
Difference in optical power between any two lanes (OMA)	DP_{OMA}			4	dBm
Peak power, each lane 40GBase-SR4	Peak			4	dBm
Transmitter and dispersion penalty (TDP), each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 TDP TDP			 3.5 3.9	 dB dB
Launch power in OMA minus TDP, each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 OMA TDP	 –6.5 –7.8			 dBm dBm
Extinction ratio	ER	3			dB
Optical return loss tolerance	RL			12	dB

3.10 Optical Receiver Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling rate, each lane			10.3125		Gbps
Center wavelengths	λ	840		860	nm
Total average power	P_{total}	–3.5		8.4	dBm
Average receive power, each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 P_{rec} P_{rec}	 –9.5		 2.4 1	 dBm dBm
Receiver power in OMA, each lane 40GBase-SR4 4x10G Base-SR compatible fanout		 –7.5 –10.7		 3	 dBm dBm
Receiver reflectance	R_{rx}			–12	dB
Stressed receiver sensitivity (OMA), each lane 40GBase-SR4 4x10G Base-SR compatible fanout	 SRS SRS			 –5.4 –7.8	 dBm dBm
Receiver jitter tolerance in OMA, each lane 40GBase-SR4				 –5.4	 dBm
Stressed receiver sensitivity test Vertical eye closure penalty (VECP), each lane Stressed eye J2 jitter, each lane Stressed eye J9 jitter, each lane OMA of each aggressor lane				 1.9 0.3 0.47 –0.4	 dB UI UI dBm
Receiver jitter tolerance test condition Jitter frequency and peak-to-peak amplitude Jitter frequency and peak-to-peak amplitude OMA of each aggressor lane				 (75, 5) (375, 1) –0.4	 (kHz, UI) (kHz, UI) dBm

3.11 Regulatory Compliance

The transceiver is RoHS 6/6 compliant and complies with international EMC (Electromagnetic Compatibility) and product safety regulations and standards

3.12 PCB Layout

Follow the guidelines given in SFF-8436.

Table 2. Regulatory Compliance

Feature	Test Method	Performance
Safety		
Product safety	UL 60950-1	UL recognized component for US and CAN
	CSA C22.2 No. 60950-1	
	EN 60950-1	TUV certificate
	IEC 60950-1	CB certificate
	Flame class V-0	Passes Needle Flame Test for component flammability verification
	Low Voltage Directive 2014/35/EU	Certified to harmonized standards listed; Declaration of Conformity issued
Laser safety	EN 60825-1, EN 60825-2	TUV certificate
	IEC 60825-1, IEC 60825-2	CB certificate
	U.S. 21 CFR 1040.10	FDA/CDRH certified with accession number
Electromagnetic compatibility		
Radiated emissions	EMC Directive 2014/30/EU	Class B digital device with a minimum -6dB margin to the limit. Final margin may vary depending on system implementation. Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less. Good system EMI design practice is required to achieve Class B margins at the system level.
	FCC rules 47 CFR Part 15	
	CISPR 22, CISPR32	
	AS/NZS CISPR22, CISPR32	
	EN 55022, EN 55032	
	ICES-003, Issue 6	
	VCCI regulations	
Immunity	EMC Directive 2014/30/EU	Certified to harmonized standards listed; Declaration of Conformity issued
	CISPR 24	
	EN 55024	
ESD	IEC/EN 61000-4-2	Exceeds Requirements. Withstands discharges of ±8kV contact, ±15kV air
Radiated immunity	IEC/EN 61000-4-3	Exceeds Requirements. Field strength of 10V/m from 80 MHz to 6 GHz. No effect on transmitter / receiver performance is detectable between these limits.
Restriction of hazardous substances (ROHS)		
RoHS	EU Directive 2011/65/EU	Compliant per the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast). A RoHS Certificate of Compliance (C of C) is available upon request. The product may use certain RoHS exemptions..

3.13 Module Outline

(Specifications are in mm unless otherwise noted.)

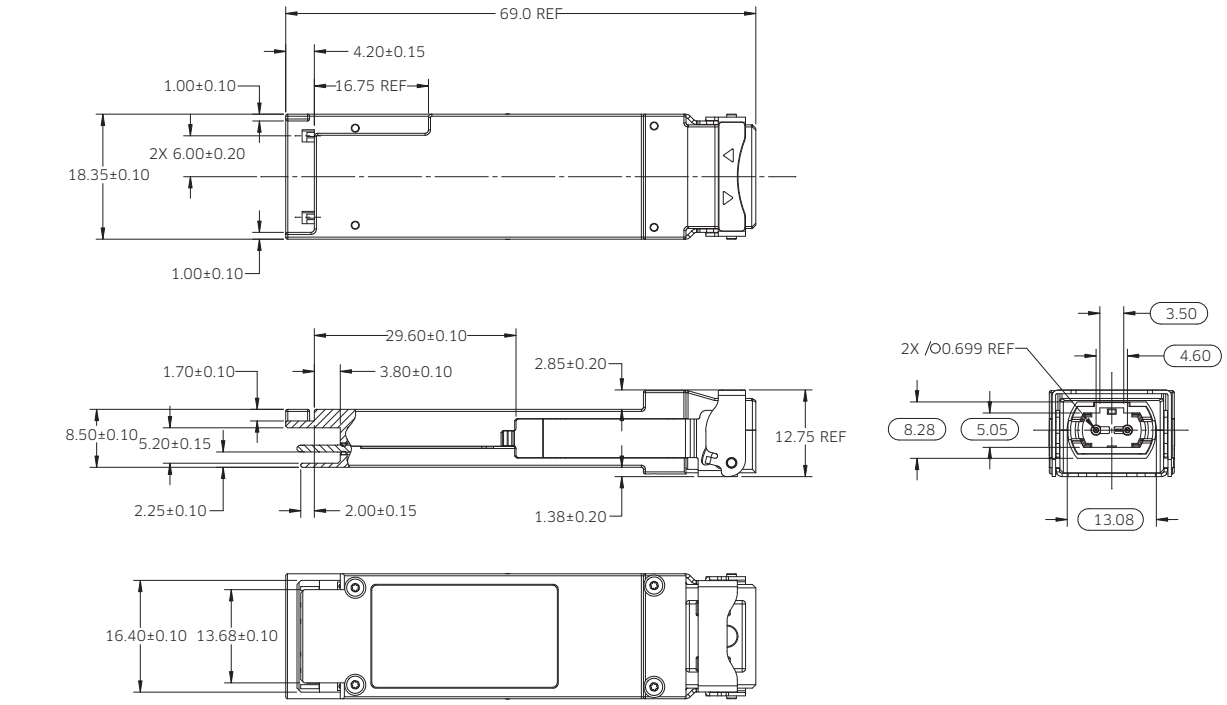


Figure 6 . JQP-04SxAx1 bail-latch version

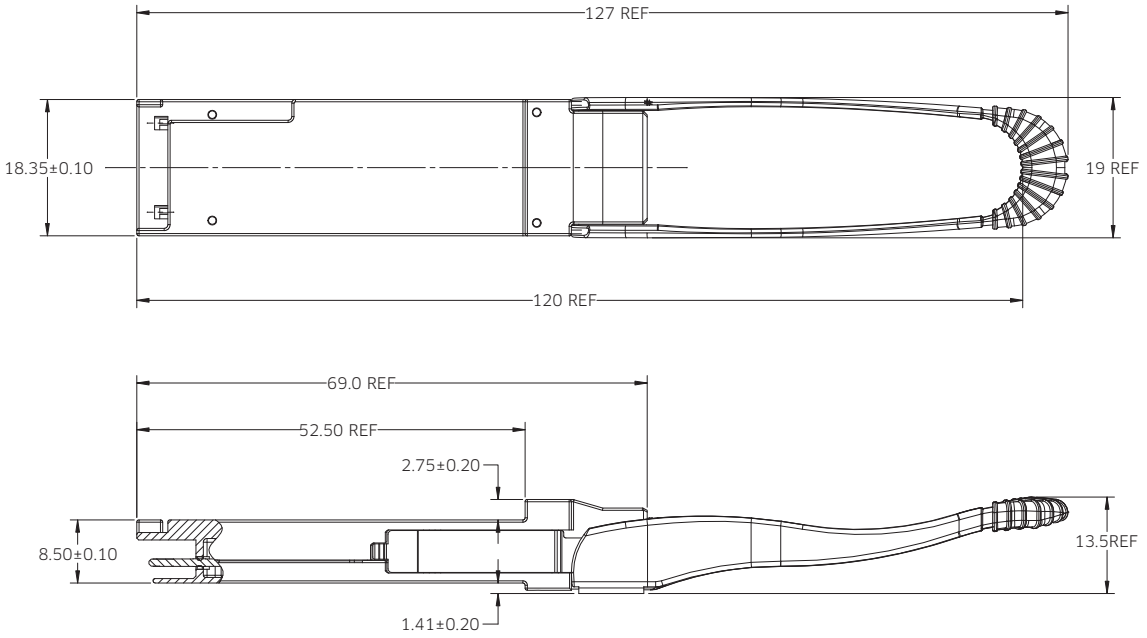
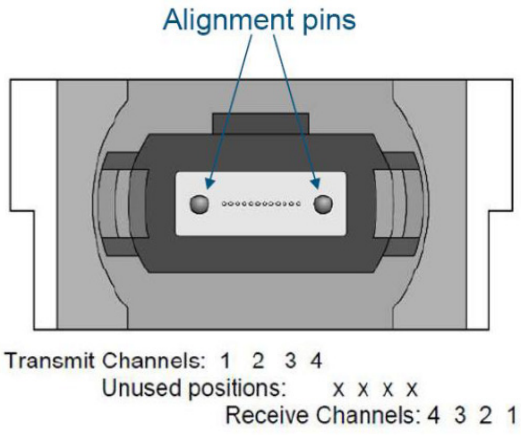


Figure 7. JQP-04SxAx2 pull-tab version

3.14 Connectors

Optical – MPO receptacle connector with an alignment key and two alignment pins



Electrical – 38-way, two-row PCB edge connector

Section 4 Related Information

Other information related to the transceiver includes:

Section 4.1 Packing and Handling Instructions

Section 4.2 Electrostatic Discharge (ESD)

Section 4.3 Laser Safety

4.1 Package and Handling Instructions

Connector Covers

The transceiver is supplied with an MPO receptacle. The connector plug supplied protects the connector during standard manufacturing processes and handling by preventing contamination from dust, aqueous solutions, body oils, or airborne particles.

Note: It is recommended that the connector plug remain on whenever the transceiver optical fiber connector is not inserted.

Recommended Cleaning and De-Greasing Chemicals

Lumentum recommends the use of methyl, isopropyl, and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (for example, trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

This product is not designed for aqueous wash.

Housing

The transceiver housing is made of zinc.

4.2 Electrostatic Discharge (ESD)

Handling

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and Operation

In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this modules receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (for example, via a serializer/deserializer chip).

4.3 Laser Safety

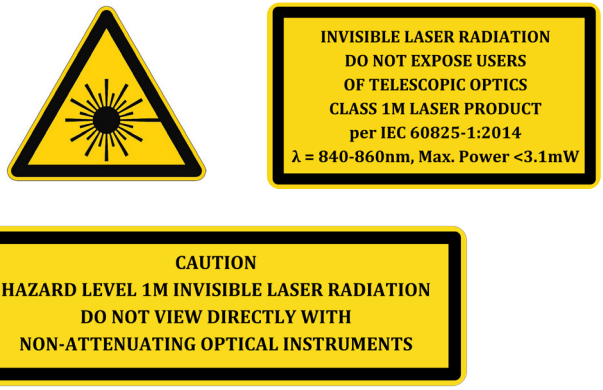
The transceiver is certified as a Class 1M (JQP-04SWAAx) or Class 1 (JQP-04SRABx) laser product per international standard IEC 60825-1:2014 3rd edition and is considered non-hazardous when operated within the limits of this specification and in accordance with the laser safety notices below.

The maximum emitted beam divergence of a Class 1M (JQP-04SWAAx) or Class 1 (JQP-04SRABx) laser product is 23° full angle from the device optical output.

This device complies with 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50.

Where the transceiver is used within an optical fiber communication system (OFCS) per the requirements of international standard IEC/EN 60825-2, the installation of this transceiver is required to be within a restricted access location based on the Class 1M (JQP-04SWAAx) or Class 1 (JQP-04SRABx) laser output power rating of the transceiver. Additionally, upon installation a Hazard Level 1M (JQP-04SWAAx) or 1 (JQP-04SRABx) marking is required to be provided as shown in the caution graphic for the transceiver or group of transceivers.

JQP-04SWAAx



JQP-04SRABx

Caution

Operating this product in a manner inconsistent with intended usage and specifications may result in hazardous radiation exposure.

Use of controls or adjustments or performance of procedures other than these specified in this product datasheet may result in hazardous radiation exposure.

Tampering with this laser product or operating this product outside the limits of this specification may be considered an 'act of manufacturing' and may require recertification of the modified product.

Viewing the laser output with certain optical instruments (for example, eye loupes, magnifiers, microscopes) within a distance of 100 mm may pose an eye hazard.

Ordering Information

For more information on this or other products and their availability, please contact your local Lumentum account manager or Lumentum directly at customer.service@Lumentum.com.

Description	Product Code
QSFP+ 40 G 40GBase-SR4, 850 nm, commercial temperature range, 100 m optical transceiver, bail latch	JQP-04SWAA1 - JDSU branded
QSFP+ 4 x 10GBase-SR compatible, 850 nm, commercial temperature range, 100 m optical transceiver, bail latch	JQP-04SRAB1 - JDSU branded
QSFP+ 40 G 40GBase-SR4, 850 nm, commercial temperature range, 100 m optical transceiver, pull tab	JQP-04SWAA2 - JDSU branded
QSFP+ 4 x 10GBase-SR compatible, 850 nm, commercial temperature range, 100 m optical transceiver, pull tab	JQP-04SRAB2 - JDSU branded

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