ASR6500S

Datasheet

Version 1.1.0

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About This Document

This document introduces the specifications of ASR6500S serial SiP modules.

Intended Readers

This document is mainly for engineers who use this module to develop their own platform and products, for instance:

- PCB Hardware Development Engineer
- Software Engineer
- Technical Support Engineer

Included Product Names

The product names corresponding to this document are as follows.

Product Name	Crystal Oscillator	Package	Frequency
ASR6500SHT	TCXO	LGA 8x8 mm	868 ~ 928 MHz
ASR6500SLT	TCXO	LGA 8x8 mm	433 ~ 510 MHz
ASR6500SL	XO	LGA 8x8 mm	433 ~ 510 MHz
ASR6500SLC	XO	LGA 8x8 mm	433 ~ 510 MHz

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ASR Microelectronics Co., Ltd.

Address: 9F, Building 10, No. 399 Keyuan Road, Zhangjiang High-tech Park, Pudong New Area, Shanghai, 201203, China

Homepage: http://www.asrmicro.com/asrweb/

Revision History

Date	Version	Release Notes
2019.10	V0.1	First Release.
2019.12	V0.2	● Update ASR6500S Package information. ● Update ASR6500S Pin definition.
2019.12	V0.3	Update ASR6500S Dimension.
2020.09	V1.1.0	Update the specifications for ASR6500SLC.

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1. Overview

1.1 General

ASR6500S is a family of LoRa SIP modules integrated with RF front end and LoRa radio transceiver SX1262 series, which supports LoRa® and FSK modulation. LoRa technology is a spread spectrum protocol optimized for low data-rate, ultra-long range and ultra-low power communication for LPWAN application.

ASR6500S is designed for long battery life with 4.2 mA of active receive current consumption, and the maximum transmit power is up to +22 dBm. The module achieves high sensitivity to -148 dBm, which provides high interference immunity for all kinds of application scenarios.

ASR6500S uses LGA package with a very small size of 8x8x1.3 mm.

1.2 Key Features

- Small footprint: 8x8x1.3 mm
- RF front end integrated
- LoRa Radio Transceiver SX1262 series
- Frequency Range:
  - 433/470 ~ 510 MHz (SL/SLT/SLC)
  - 868 ~ 928 MHz (SHT)
- Embedded Crystal Type:
  - XO (SL/SLC)
  - TCXO (SLT/SHT)
- Maximum Power: up to 22 dBm at LoRa CW
- LoRa High sensitivity:
  - -148 dBm at BW=10.4 KHz, SF12. (SL/SLT/SHT)
  - -129 dBm at BW=125 KHz, SF9 (SLC)
  - -129 dBm at BW=250 KHz, SF10 (SLC)
- Maximum Link Budget:
  - 170 dB at BW=10.4 KHz, SF12 (SL/SLT/SHT)
  - 151 dB at BW=125 KHz, SF9 (SLC)

- Programmable Bit rate LoRa:
  - Max 62.5 Kbps at BW=500 KHz, SF5
  - Min 0.018 Kbps at BW=7.8 KHz, SF12 (SL/SLT/SHT)
  - Min 1.76 Kbps at BW=125 KHz, SF9 (SL/SLT/SHT)
- Programmable bit rate GFSK up to 300 Kbps
- Preamble detection
- 135 dB Dynamic Range RSSI
- Excellent Blocking Immunity
- Automatic RF Sense and CAD with Ultra-Fast AFC

1.3 Block Diagram

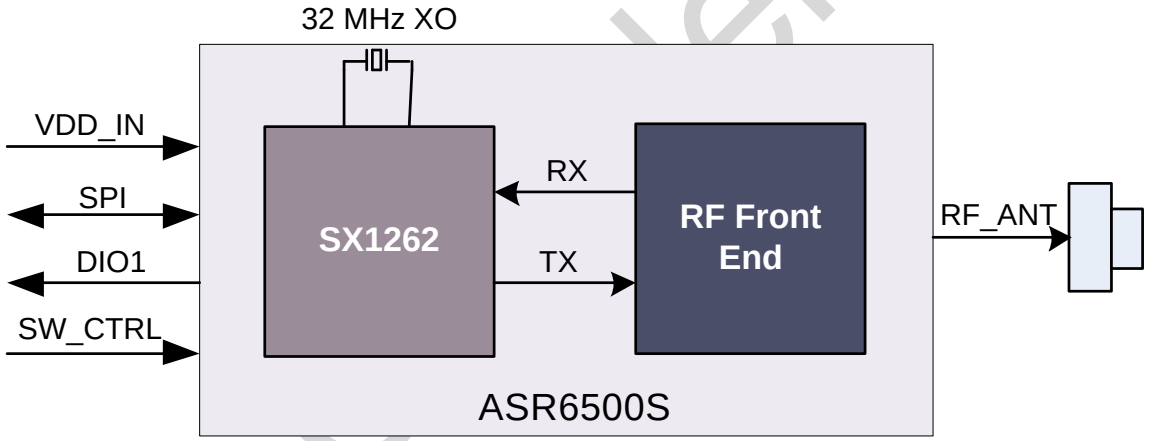


Figure 1-1 Block Diagram of ASR6500S Module

1.4 Part Number Information

The following table shows the part number information of ASR6500S family.

Table 1-1 Part Number Information

Part Number	Crystal Oscillator	Frequency	Pin Number	Package
ASR6500SHT	TCXO	868 ~ 928 MHz	13	LGA 8x8 mm
ASR6500SLT	TCXO	433 ~ 510 MHz	13	LGA 8x8 mm
ASR6500SL	XO	433 ~ 510 MHz	13	LGA 8x8 mm
ASR6500SLC	XO	433 ~ 510 MHz	13	LGA 8x8 mm

1.5 Specification

Table 1-2 shows the general specifications of ASR6500S SIP module.

Table 1-2 General Specifications of ASR6500S Module

Item	Description
Product description	LoRa Wireless Communication Module
Host Interface	SPI
Operation Conditions:	
Temperature	● Storage: -55 ~ +125℃ ● Operating: -40 ~ +85℃
Humidity	● Storage: 5 ~ 95% (Non-Condensing) ● Operating: 10 ~ 95% (Non-Condensing)
Dimension	8x8x1.3 mm
Package	LGA Type

1.6 Applications

ASR6500S SIP module integrated with SX1262 series enables new generation of IoT applications.

- Smart meters
- Supply chain and logistics
- Building automation
- Agricultural sensors
- Smart cities
- Retail store sensors
- Asset tracking
- Streetlights
- Parking sensors
- Environmental sensors
- Healthcare
- Safety and security sensors
- Remote control applications

2. Electrical Characteristics

Electrical characteristics include *absolute maximum rating*, *recommended operating range* and *power consumption characteristics* for the module.

2.1 Absolute Maximum Rating

Table 2-1 Absolute Maximum Rating

Parameter	Symbol	Min.	Typ.	Max.	Unit
RF Supply Voltage	VDD_IN	-0.3		3.9	V
RF Input level	Pin			+10	dBm

2.2 Recommended Operating Range

Table 2-2 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	1.8	3.3	3.7	V
RF Input Power	Pin			+10	dBm

2.3 Power Consumption Characteristics

Table 2-3 Power Consumption Characteristics

Symbol	Mode	Conditions	Min.	Typ.	Max.	Unit
IDD_OFF	OFF mode (SLEEP mode with code start)	All blocks off	-	160	-	nA
IDD_SL	SLEEP mode (SLEEP mode with warm start)	RF Config Retained; Config retained + RC64k	- -	600 1.2	- -	nA uA
IDD_SBR	STDBY_RC mode	RC13M, XOSC OFF	-	0.6	-	mA
IDD_SBX	STDBY_XOSC mode	XOSC ON	-	0.8	-	mA
IDD_FS	Synthesizer mode	DC-DC mode used LDO mode used	- -	2.1 3.55	- -	mA mA
IDD_RX	Receive mode (DC-DC mode used)	FSK 4.8 Kbps	-	4.2	-	mA
		LoRa 125 KHz	-	4.6	-	mA
		Rx Boosted, FSK 4.8 Kbps	-	4.8	-	mA
		Rx Boosted, 125 KHz	-	5.3	-	mA
	Receive mode (LDO mode used)	FSK 4.8 Kbps	-	8	-	mA
		LoRa 125 KHz	-	8.8	-	mA
		Rx Boosted, FSK 4.8 Kbps	-	9.3	-	mA
		Rx Boosted, 125 KHz	-	10.1	-	mA
IDD_TX	Transmit mode (433/470~510 MHz)	Pout = +22 dBm	-	108	-	mA
		Pout = +20 dBm	-	90	-	mA
		Pout = +17 dBm	-	75	-	mA
		Pout = +14 dBm	-	63	-	mA
	Transmit mode (868~928 MHz)	Pout = +22 dBm	-	118	-	mA
		Pout = +20 dBm	-	102	-	mA
		Pout = +17 dBm	-	95	-	mA
		Pout = +14 dBm	-	90	-	mA

2.4 General Characteristics

- Digital Modem Bank for ASR6500SL/ASR6500SLT/ASR6500SHT:
  - LoRa® Rx/Tx, BW = 7.8 - 500 KHz, SF5 to SF12, BR = 0.018 - 62.5 Kbps
  - (G)FSK Rx/Tx, with BR = 0.6 - 300 Kbps
- Digital Modem Bank for ASR6500SLC:
  - LoRa® Rx/Tx, BW = 125 -250 - 500 KHz
  - LoRa® SF = 5 - 6 - 7 - 8 - 9 for BW = 125 KHz
  - LoRa® SF = 5 - 6 - 7 - 8 - 9 - 10 for BW = 250 KHz
  - LoRa® SF = 5 - 6 - 7 - 8 - 9 - 10 - 11 for BW = 500 KHz
  - (G)FSK Rx/Tx, with BR = 0.6 - 300 Kbps

2.5 RF Characteristics

Table 2-4 gives the electrical specifications for the LoRa RF transceiver operating with LoRa modulation.

Unless otherwise specified, the following conditions apply:

- Supply Voltage = 3.3 V
- Temperature = 25℃
- Frequency bands: 470 MHz
- Bandwidth (BW) = 10.4/125/250/500 KHz
- Spreading Factor (SF) = 12
- Coding Rate (CR) = 4/6
- Package Error Rate (PER) = 1%
- CRC on payload enabled
- Payload length = 10 Bytes
- Preamble Length = 12 symbols
- With matched impedances

Table 2-4 LoRa RF Receiver Characteristics

Items	Condition	SL&SLC	SHT (Typ.)	SHT (Typ.)	Unit
Frequency Range		470	868	915	MHz
Sensitivity	BW = 10.4 KHz, SF = 12	-148	-148	-148	dBm
	BW = 10.4 KHz, SF = 7	-134	-134	-134	dBm
	BW = 125 KHz, SF = 12	-138	-138	-138	dBm
	BW = 125 KHz, SF = 7	-124	-124	-124	dBm
	BW = 250 KHz, SF = 12	-134	-134	-134	dBm
	BW = 250 KHz, SF = 7	-121	-121	-121	dBm
	BW = 500 KHz, SF = 12	-129	-129	-129	dBm
	BW = 500 KHz, SF = 7	-117	-117	-117	dBm
2^{nd} order harmonic	Tx Power = 22 dBm	-41.55	-51.25	-51.25	dBm
3^{rd} order harmonic	Tx Power = 22 dBm	-42.65	-40.12	-37.12	dBm
4^{th} order harmonic	Tx Power = 22 dBm	-55.35	-41.64	-40.80	dBm
5^{th} order harmonic	Tx Power = 22 dBm	-55.33	-41.65	-44.65	dBm

2.6 Digital Characteristics

2.6.1 DC Characteristics

Table 2-5 Digital IO Specification

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
VIH	I/O input high level		0.7xVDD			V
VIL	I/O input low level				0.3xVDD	V
RPU	Weak pull up resistor	Vin=GND	30	45	60	KΩ
RPD	Weak pull down resistor	Vin=VDD	30	45	60	KΩ

2.6.2 RST Characteristics

Figure 2-1 shows the recommended XRES pin connection. An external RESET button is used to generate reset pulse of the whole module. The 0.1uF capacitor is to filter out the parasitic reset glitch.

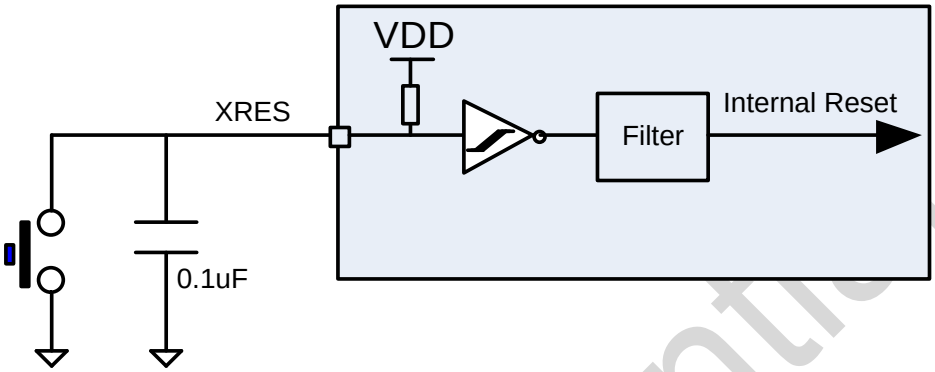


Figure 2-1 XRES Pin Connection

3. Pin Connection

3.1 I/O Description

Table 3-1 ASR6500S Pinout in LGA 8x8

Pin No.	Pin Name	P/G/I/O	Description
1	DIO1	I/O	General purpose I/O
2	SPI_BUSY	I/O	SPI busy indicator
3	SPI_NRESET	I/O	SPI reset, active low
4	GND	P	GND
5	RF_ANT	I/O	Antenna connector
6	SW_CTRL	I/O	RFSW control
7	SPI_MISO	I/O	SPI slave output
8	SPI_MOSI	I/O	SPI slave input
9	SPI_SCK	I/O	SPI clock
10	SPI_NSS	I/O	SPI slave select
11	VDD_IN	P	Input voltage
12	PGND	P	DC-DC GND, Connect to GND external
13	GND	P	GND

3.2 Pin Assignment

Pin assignment of ASR6500S SIP modules is shown in the following diagram (top view).

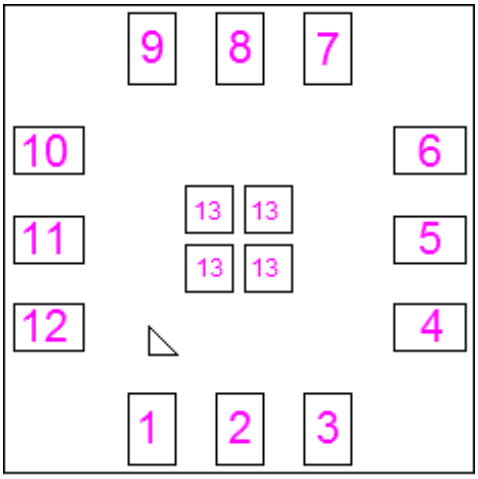
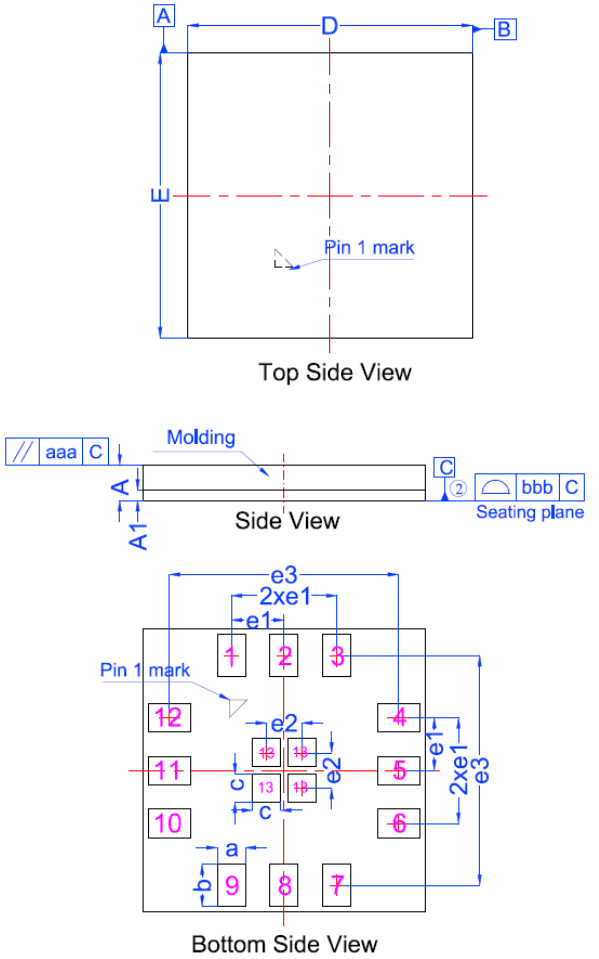


Figure 3-1 Pin Assignment of ASR6500S

4. Package Information



DIMENSIONAL REFERENCES *Units:mm*

SYMBOL	DIMENSIONAL REQMTS			SYMBOL	Tolerance of Form &Position
	MIN	NOM	MAX	aaa	0.10
A	1.26	1.30	1.34	bbb	0.10
A1	0.27	0.30	0.33		
D	7.90	8.00	8.10		
E	7.90	8.00	8.10		
a	0.75	0.80	0.85		
b	1.15	1.20	1.25		
c	0.75	0.80	0.85		
e1	1.50 REF				
e2	1.00 REF				
e3	6.50 REF				

Note:

1. All dimensions are in mm
2. Datum 'C' is the mounting surface, with which the package is in contact

PIN	Value	PIN	Value
1	DIO1	8	SPI_MOSI
2	SPI_BUSY	9	SPI_SCK
3	SPI_NRST	10	SPI_NSS
4	GND	11	VDD_IN
5	RF_ANT	12	PGND
6	SW_CTRL	13	GND
7	SPI_MISO		

Figure 4-1 ASR6500S Package Outline Drawing